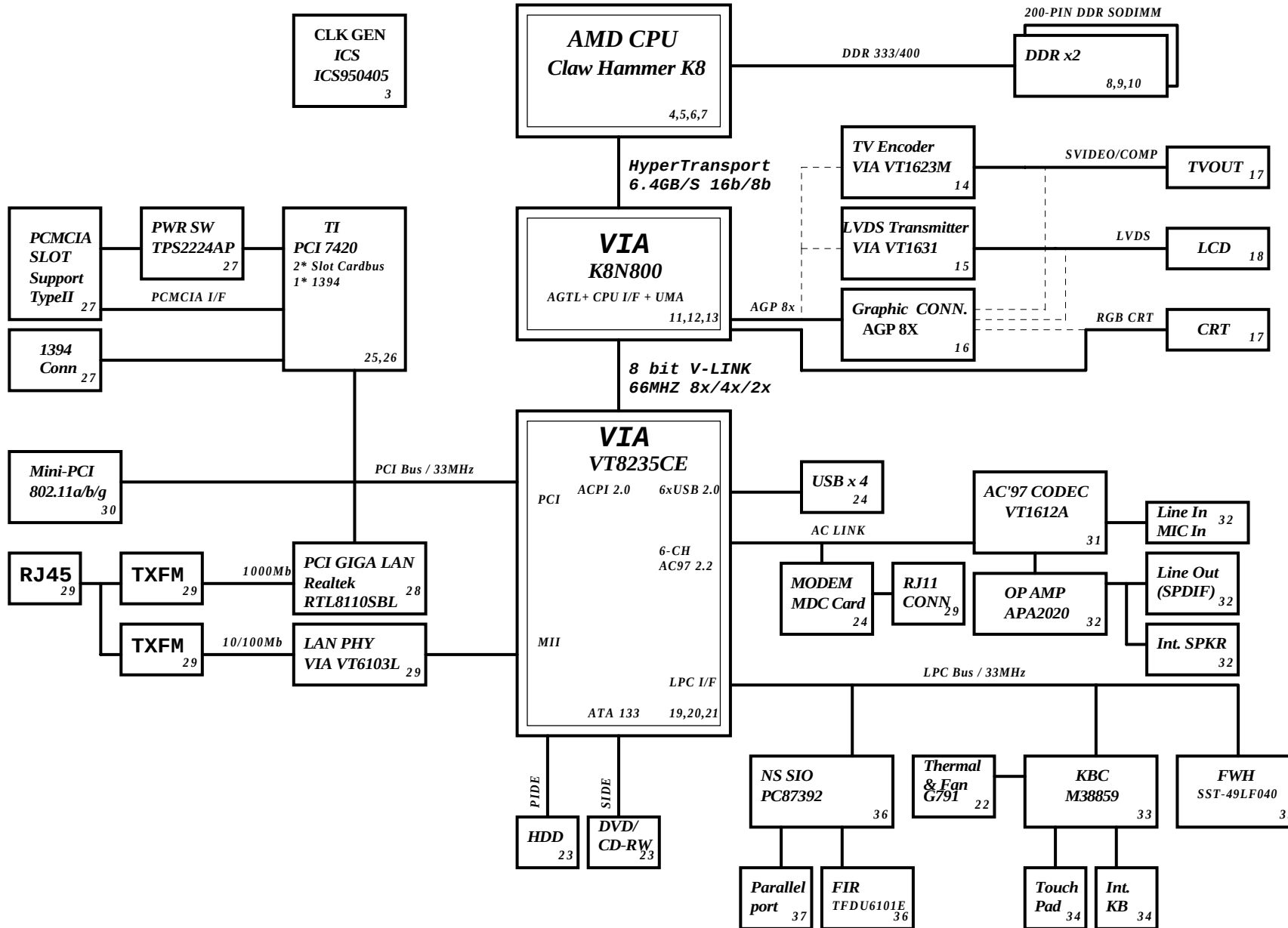


EGRET Block Diagram



PCB Layer Stackup
L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

Battery Charger		46
MAX1645BEEI		
INPUTS	OUTPUTS	
AD+ BAT+	DCBATOUT	
SYSTEM DC/DC		43
MAX1999		
INPUT	OUTPUT	
DCBATOUT	5V_S5, 3D3V_S5	
SYSTEM DC/DC		44
TPS5110		
INPUT	OUTPUT	
DCBATOUT 2D5V_S3	2D5V_S3 1D5V_S0	

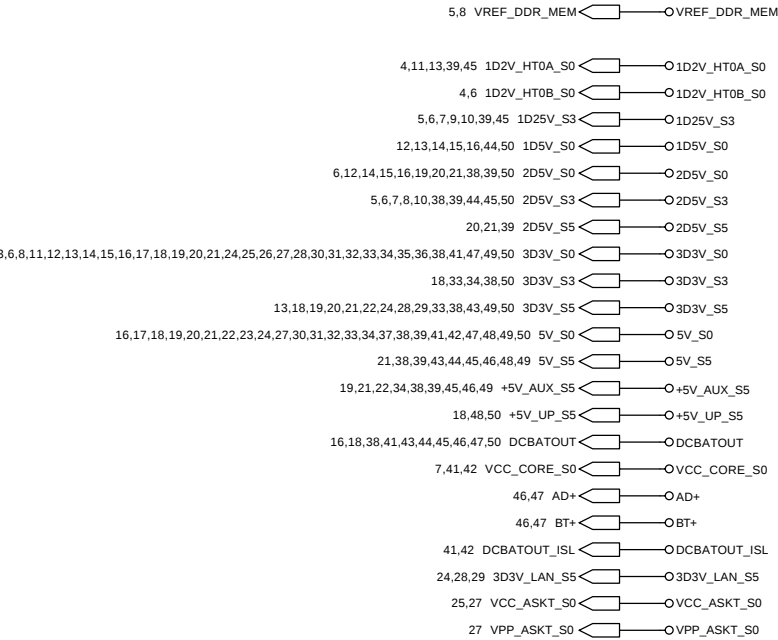
CPU V_CORE _{41,42} ISL6559CR	
INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM POWER^{44,4} FDD6035AL/FDS9412-U FDS9412-U / U14892DV/LP2951ACM APL5508 - 18VC/APL5308 - 25AC	
INPUT	OUTPUT
5V_S3 3D3V_S5 3D3V_S3 3D3V_S0 DCBATOUT	2D5V_S5 5V_S0 3D3V_S3 3D3V_S0 3D3V_LAN_S3 1D8V_S0 +5V_AUX_S5 +5V_UP_S5 2D5V_S0

EGRET REVISION HISTORY

PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
VGA & AGP		P_INTA#	
PCI7420-CardBus A	AD22	P_INTB#	P_REQ#1/P_GNT#1
PCI7420-CardBus B	AD22	P_INTC#	P_REQ#1/P_GNT#1
PCI7420-IEEE1394A	AD22	P_INTD#	P_REQ#1/P_GNT#1
Mini-PCI	AD21	P_INTF#	P_REQ#0/P_GNT#0
Giga LAN RTL8110SBL	AD23	P_INTG#	P_REQ#2/P_GNT#2



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
REVISION HISTORY		
Size A3	Document Number EGRET	Rev SC
Date: Friday, July 23, 2004		
Sheet 2 of 50		

By KDS suggested change
From 78.33034.1B1
To 78.12034.1B1

GUICLK Damping only
Stuff for K8N800 UMA

FS0~FS2 Have internal Pull-up resistor
FS3 Have internal Pull-down resistor

Library Issue
Pin32: PD#

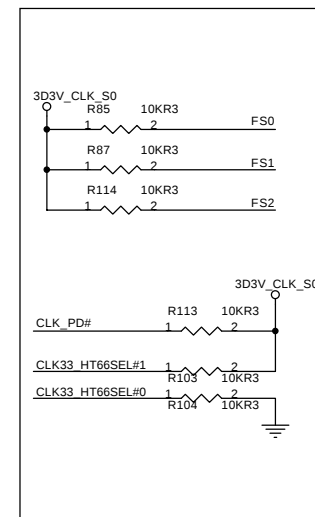
CLK33_LAN Damping only
Stuff for RTL8110SB

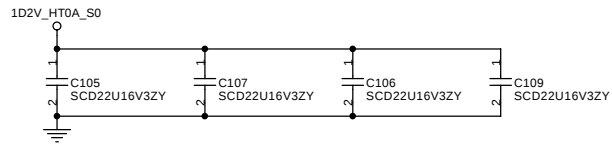
CLK66_VGA Damping only
Stuff for K8N800 Discrete

Input Configuration				Clock Generator Output			
FS3	FS2	FS1	FS0	CPU (MHz)	PCI33_HT66 (MHz)	PCI33 (MHz)	
0	0	0	0	100.90	67.27	33.63	All output Tri-state
0	0	0	1	133.90	66.95	33.48	
0	0	1	0	168.00	67.20	33.60	
0	0	1	1	202.00	67.33	33.67	
0	1	0	0	100.20	66.80	33.40	
0	1	0	1	133.50	66.75	33.38	
0	1	1	0	166.70	66.68	33.34	
0	1	1	1	200.40	66.80	33.40	Normal Hammer operation
1	0	0	0	150.00	60.00	30.00	
1	0	0	1	180.00	60.00	30.00	
1	0	1	0	210.00	70.00	35.00	
1	0	1	1	240.00	60.00	30.00	
1	1	0	0	270.00	67.50	33.75	
1	1	0	1	233.33	66.67	33.33	
1	1	1	0	266.67	66.67	33.33	
1	1	1	1	300.00	75.00	37.50	

24_48 SEL#	24_48MHz
0	48MHz
1	24MHz

PCIHT66 SEL[1:0]#		PCI33_HT66[3:0]		
SEL0	SEL1	PIN7	PIN8	PIN11
0	0	HT66	HT66	PCI33
0	1	HT66	HT66	HT66
1	0	PCI33	PCI33	PCI33
1	1	HT66	PCI33	PCI33



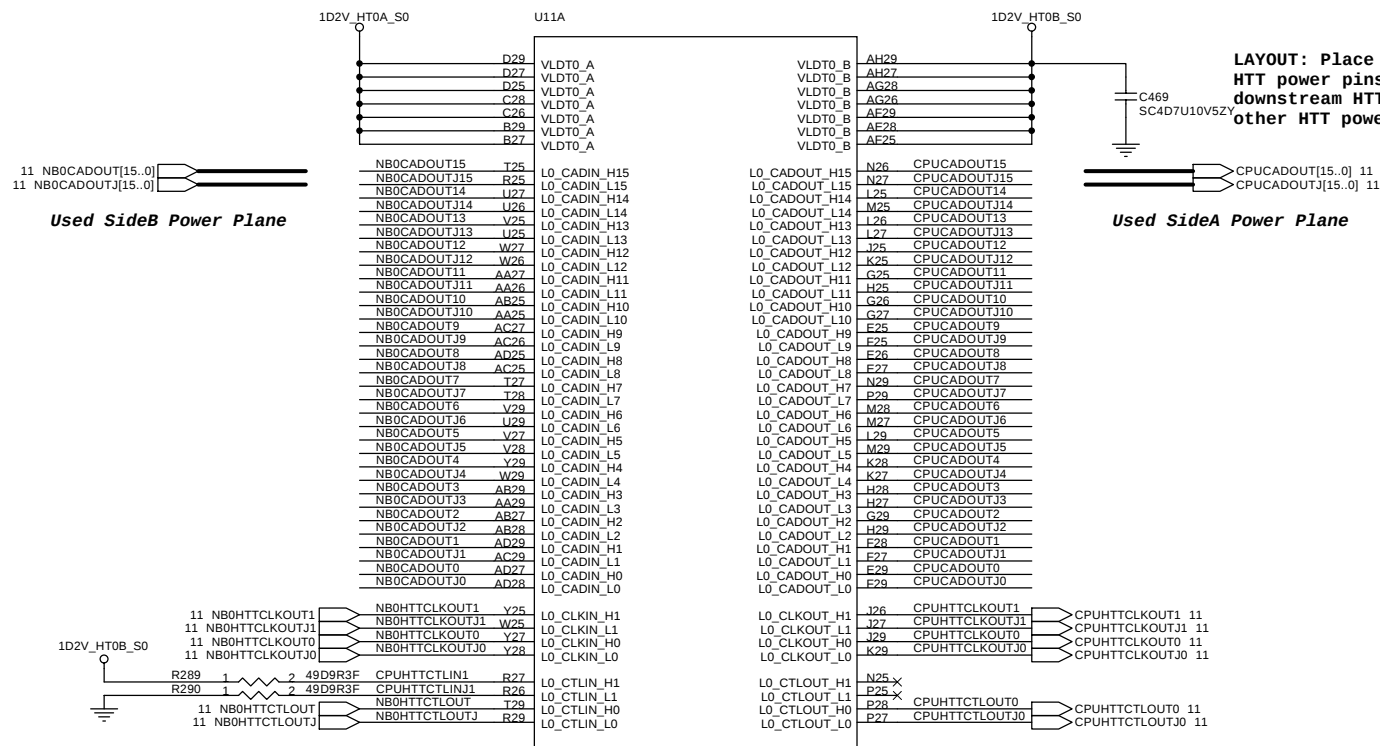


11,13,39,45 1D2V_HT0A_S0

6 1D2V_HT0B_S0

HTT for CPU sideA
Transmit power
and NB sideA Receive
power

HTT for CPU sideB
Receive power
and NB sideA
Transmit power

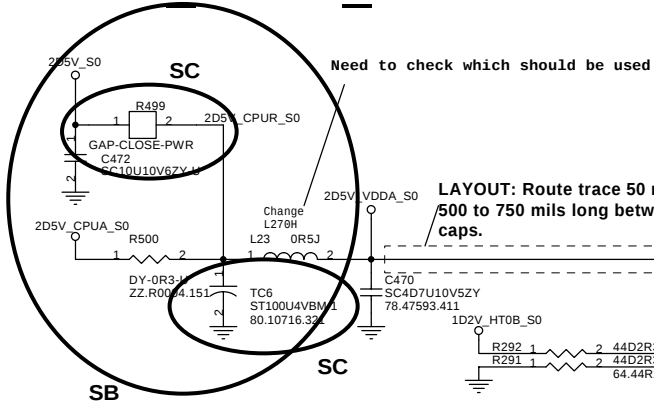


BGA754-SKT-U
62.10030.041

By ME request U11 P/N:
Main 62.10030.041
Second 62.10053.191
Third 62.10053.201

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
CPU(1/4) HyperTransport I/F		
Size	Document Number	Rev
A3	EGRET	SC
Date: Friday, July 23, 2004		Sheet 4 of 50

2D5V VDDA_S0



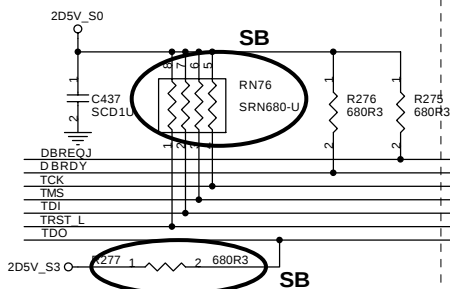
KEMET, NT: 5.7, B2 size
ST100U4VBM-1 (80.10716.321)
Iripple=1.1A, ESR=70mohm
SANYO, NT: 6.1
Iripple=1.1A, ESR=70mohm
3.5/2.8/2.0
77.21071.031

LAYOUT: Route trace 50 mils wide and 500 to 750 mils long between these caps.

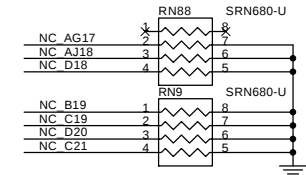
LAYOUT: Route VDDA trace approx. 50 mils wide (use 2x25 mil traces to exit ball field) and 500 mils long.

AMD suggest voltage from 2D5V_S0 to 2D5V_S3 differentially impedance 100

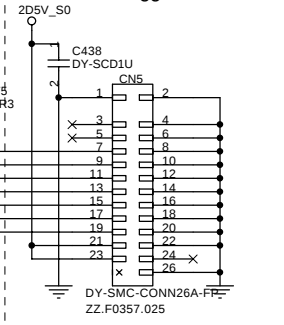
HDT Connectors



CHANGE FROM 1KR3 TO 680R2 FOR AMD CHECK LIST



Add HDT connector for AMD suggested

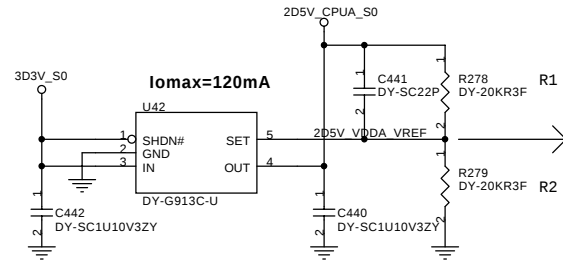


Validation Test Points

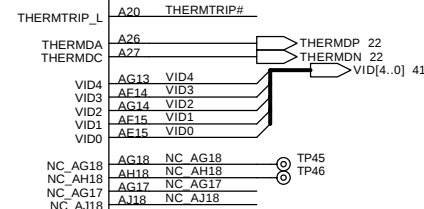
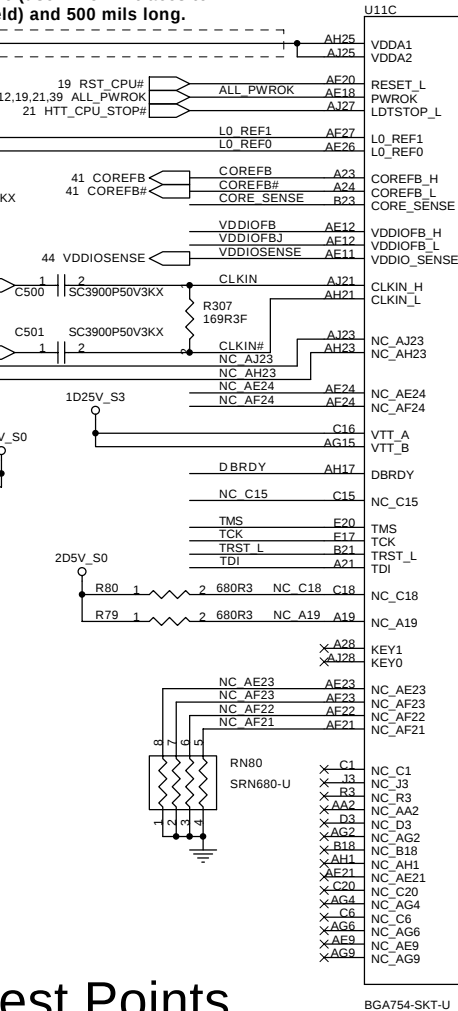
LAYOUT: Place close to the CPU.

NC C15 TP36
 NC AE23 TP24
 NC AF23 TP25
 NC AF22 TP26
 NC AF21 TP27

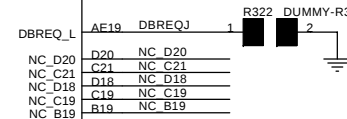
RST_CPU# TP30
 CLKIN TP32
 CLKIN# TP33
 CORE_SENSE TP28
 VDDIOFB TP43
 VDDIOFB# TP44
 VDDIOSENSE TP41
 NC AE24 TP29
 NC AF24 TP31



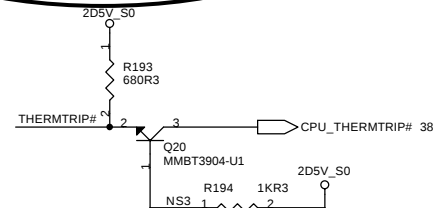
$$V_{out} = 1.25 * (1 + R1/R2)$$



LAYOUT: Route FBCLKOUT_H/L differentially impedance 80



Connect to VDDIO for AMD suggest.

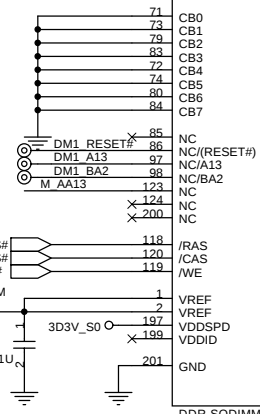


THERMTRIPJ Level shift to VT8235 EM_OFF PIN near VT8235

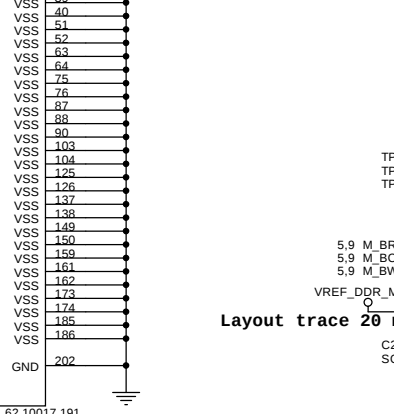
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU(3/4) Control & Debug		
Size	Document Number	Rev
A3	EGRET	SC
Date: Friday, July 23, 2004	Sheet 6 of 50	

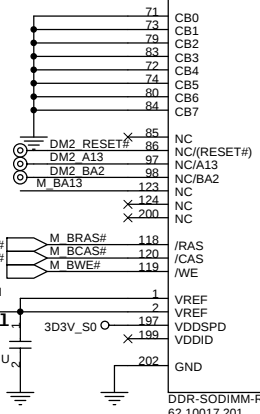
M_AA0	112	A0
M_AA1	111	A1
M_AA2	110	A2
M_AA3	109	A3
M_AA4	108	A4
M_AA6	107	A5
M_AA5	106	A6
M_AA7	105	A7
M_AA8	102	A8
M_AA9	101	A9
M_AA10	115	A10 / AP
M_AA11	100	A11
M_AA12	99	A12
M_ABS#0	117	BA0
M_ABS#1	116	BA1
M_DATA R 0	5	DQ0
M_DATA R 1	7	DQ1
M_DATA R 2	13	DQ2
M_DATA R 3	17	DQ3
M_DATA R 4	6	DQ4
M_DATA R 5	8	DQ5
M_DATA R 6	14	DQ6
M_DATA R 7	18	DQ7
M_DATA R 8	19	DQ8
M_DATA R 9	23	DQ9
M_DATA R 10	29	DQ10
M_DATA R 11	31	DQ11
M_DATA R 12	20	DQ12
M_DATA R 13	24	DQ13
M_DATA R 14	30	DQ14
M_DATA R 15	32	DQ15
M_DATA R 16	41	DQ16
M_DATA R 17	43	DQ17
M_DATA R 18	49	DQ18
M_DATA R 19	53	DQ19
M_DATA R 20	42	DQ20
M_DATA R 21	44	DQ21
M_DATA R 22	50	DQ22
M_DATA R 23	54	DQ23
M_DATA R 24	55	DQ24
M_DATA R 25	59	DQ25
M_DATA R 26	65	DQ26
M_DATA R 27	67	DQ27
M_DATA R 28	56	DQ28
M_DATA R 29	60	DQ29
M_DATA R 30	66	DQ30
M_DATA R 31	68	DQ31
M_DATA R 32	127	DQ32
M_DATA R 33	129	DQ33
M_DATA R 34	135	DQ34
M_DATA R 35	139	DQ35
M_DATA R 36	128	DQ36
M_DATA R 37	130	DQ37
M_DATA R 38	136	DQ38
M_DATA R 39	140	DQ39
M_DATA R 40	141	DQ40
M_DATA R 41	145	DQ41
M_DATA R 42	151	DQ42
M_DATA R 43	153	DQ43
M_DATA R 44	142	DQ44
M_DATA R 45	146	DQ45
M_DATA R 46	152	DQ46
M_DATA R 47	154	DQ47
M_DATA R 48	163	DQ48
M_DATA R 49	165	DQ49
M_DATA R 50	171	DQ50
M_DATA R 51	175	DQ51
M_DATA R 52	164	DQ52
M_DATA R 53	166	DQ53
M_DATA R 54	172	DQ54
M_DATA R 55	176	DQ55
M_DATA R 56	177	DQ56
M_DATA R 57	181	DQ57
M_DATA R 58	187	DQ58
M_DATA R 59	189	DQ59
M_DATA R 60	178	DQ60
M_DATA R 61	182	DQ61
M_DATA R 62	188	DQ62
M_DATA R 63	190	DQ63



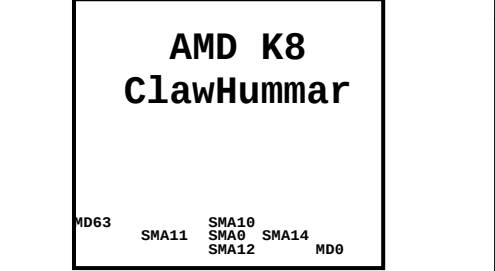
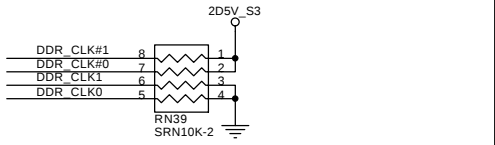
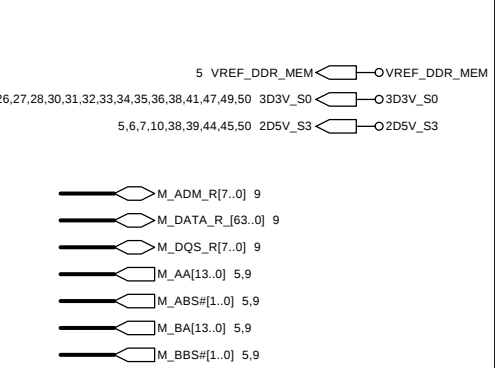
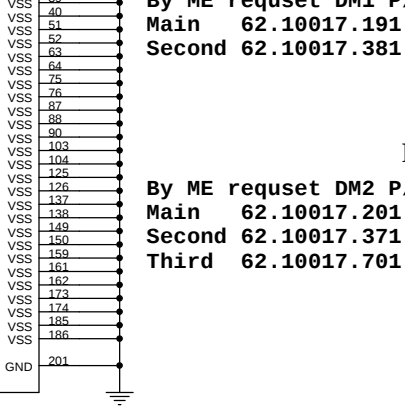
/CS0	121	M_CS#0 5,9
/CS1	122	M_CS#1 5,9
CKE0	96	M_CKE#0 5,9
CKE1	95	
DQS0	11	M_DQS_R0
DQS1	25	M_DQS_R1
DQS2	47	M_DQS_R2
DQS3	61	M_DQS_R3
DQS4	133	M_DQS_R4
DQS5	147	M_DQS_R5
DQS6	169	M_DQS_R6
DQS7	183	M_DQS_R7
DQS8	77	
DM0	12	M_ADM_R0
DM1	26	M_ADM_R1
DM2	48	M_ADM_R2
DM3	62	M_ADM_R3
DM4	148	M_ADM_R5
DM5	170	M_ADM_R6
DM6	184	M_ADM_R7
DM7		
DM8		
CK0	35	M_CLK5 5,9
/CK0	37	
CK1	160	M_CLK#5 5,9
/CK1	158	M_CLK#7 5,9
CK2	89	DDR_CLK#0
/CK2	91	DDR_CLK#0
SCL	195	SMBC_SB
SDA	193	SMBD_SB
SA0	194	
SA1	196	
SA2	198	
VDD	9	
VDD	10	
VDD	21	
VDD	22	
VDD	33	
VDD	34	
VDD	36	
VDD	45	
VDD	46	
VDD	57	
VDD	58	
VDD	69	
VDD	70	
VDD	81	
VDD	82	
VDD	92	
VDD	93	
VDD	94	
VDD	113	
VDD	114	
VDD	131	
VDD	132	
VDD	143	
VDD	144	
VDD	155	
VDD	156	
VDD	157	
VDD	167	
VDD	168	
VDD	179	
VDD	180	
VDD	191	
VDD	192	
VSS	3	
VSS	4	
VSS	15	
VSS	16	
VSS	27	
VSS	28	
VSS	38	
VSS	39	
VSS	40	
VSS	51	
VSS	52	
VSS	63	
VSS	64	
VSS	75	
VSS	76	
VSS	87	
VSS	88	
VSS	90	
VSS	103	
VSS	104	
VSS	125	
VSS	126	
VSS	137	
VSS	138	
VSS	149	
VSS	150	
VSS	159	
VSS	161	
VSS	162	
VSS	173	
VSS	174	
VSS	185	
VSS	186	
VSS	202	



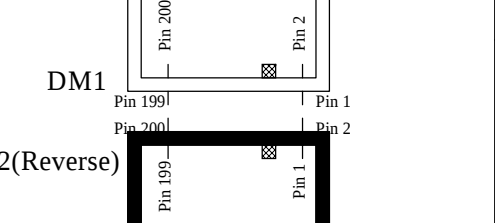
M_BA0	112	A0
M_BA1	111	A1
M_BA2	110	A2
M_BA3	109	A3
M_BA4	108	A4
M_BA6	107	A5
M_BA5	106	A6
M_BA7	105	A7
M_BA8	102	A8
M_BA9	101	A9
M_BA10	115	A10 / AP
M_BA11	100	A11
M_BA12	99	A12
M_BBS#0	117	BA0
M_BBS#1	116	BA1
M_DATA R 0	5	DQ0
M_DATA R 1	7	DQ1
M_DATA R 2	13	DQ2
M_DATA R 3	17	DQ3
M_DATA R 4	6	DQ4
M_DATA R 5	8	DQ5
M_DATA R 6	14	DQ6
M_DATA R 7	18	DQ7
M_DATA R 8	19	DQ8
M_DATA R 9	23	DQ9
M_DATA R 10	29	DQ10
M_DATA R 11	31	DQ11
M_DATA R 12	20	DQ12
M_DATA R 13	24	DQ13
M_DATA R 14	30	DQ14
M_DATA R 15	32	DQ15
M_DATA R 16	41	DQ16
M_DATA R 17	43	DQ17
M_DATA R 18	49	DQ18
M_DATA R 19	53	DQ19
M_DATA R 20	42	DQ20
M_DATA R 21	44	DQ21
M_DATA R 22	50	DQ22
M_DATA R 23	54	DQ23
M_DATA R 24	55	DQ24
M_DATA R 25	59	DQ25
M_DATA R 26	65	DQ26
M_DATA R 27	67	DQ27
M_DATA R 28	56	DQ28
M_DATA R 29	60	DQ29
M_DATA R 30	66	DQ30
M_DATA R 31	68	DQ31
M_DATA R 32	127	DQ32
M_DATA R 33	129	DQ33
M_DATA R 34	135	DQ34
M_DATA R 35	139	DQ35
M_DATA R 36	128	DQ36
M_DATA R 37	130	DQ37
M_DATA R 38	136	DQ38
M_DATA R 39	140	DQ39
M_DATA R 40	141	DQ40
M_DATA R 41	145	DQ41
M_DATA R 42	151	DQ42
M_DATA R 43	153	DQ43
M_DATA R 44	142	DQ44
M_DATA R 45	146	DQ45
M_DATA R 46	152	DQ46
M_DATA R 47	154	DQ47
M_DATA R 48	163	DQ48
M_DATA R 49	165	DQ49
M_DATA R 50	171	DQ50
M_DATA R 51	175	DQ51
M_DATA R 52	164	DQ52
M_DATA R 53	166	DQ53
M_DATA R 54	172	DQ54
M_DATA R 55	176	DQ55
M_DATA R 56	177	DQ56
M_DATA R 57	181	DQ57
M_DATA R 58	187	DQ58
M_DATA R 59	189	DQ59
M_DATA R 60	178	DQ60
M_DATA R 61	182	DQ61
M_DATA R 62	188	DQ62
M_DATA R 63	190	DQ63



/CS0	121	M_CS#2 5,9
/CS1	122	M_CS#3 5,9
CKE0	96	M_CKE#1 5,9
CKE1	95	
DQS0	11	M_DQS_R0
DQS1	25	M_DQS_R1
DQS2	47	M_DQS_R2
DQS3	61	M_DQS_R3
DQS4	133	M_DQS_R4
DQS5	147	M_DQS_R5
DQS6	169	M_DQS_R6
DQS7	183	M_DQS_R7
DQS8	77	
DM0	12	M_ADM_R0
DM1	26	M_ADM_R1
DM2	48	M_ADM_R2
DM3	62	M_ADM_R3
DM4	148	M_ADM_R5
DM5	170	M_ADM_R6
DM6	184	M_ADM_R7
DM7		
DM8		
CK0	35	M_CLK4 5,9
/CK0	37	
CK1	160	M_CLK#4 5,9
/CK1	158	M_CLK#6 5,9
CK2	89	DDR_CLK#1
/CK2	91	DDR_CLK#1
SCL	195	SMBC_SB 3,21
SDA	193	SMBD_SB 3,21
SA0	194	DM2 SA0
SA1	196	
SA2	198	
VDD	9	
VDD	10	
VDD	21	
VDD	22	
VDD	33	
VDD	34	
VDD	36	
VDD	45	
VDD	46	
VDD	57	
VDD	58	
VDD	69	
VDD	70	
VDD	81	
VDD	82	
VDD	92	
VDD	93	
VDD	94	
VDD	113	
VDD	114	
VDD	131	
VDD	132	
VDD	143	
VDD	144	
VDD	155	
VDD	156	
VDD	157	
VDD	167	
VDD	168	
VDD	179	
VDD	180	
VDD	191	
VDD	192	
VSS	3	
VSS	4	
VSS	15	
VSS	16	
VSS	27	
VSS	28	
VSS	38	
VSS	39	
VSS	40	
VSS	51	
VSS	52	
VSS	63	
VSS	64	
VSS	75	
VSS	76	
VSS	87	
VSS	88	
VSS	90	
VSS	103	
VSS	104	
VSS	125	
VSS	126	
VSS	137	
VSS	138	
VSS	149	
VSS	150	
VSS	159	
VSS	161	
VSS	162	
VSS	173	
VSS	174	
VSS	185	
VSS	186	
VSS	201	



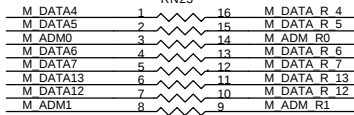
DDR SOCKET PLACEMENT
TOP VIEW PERSPECTIVE DRAWING



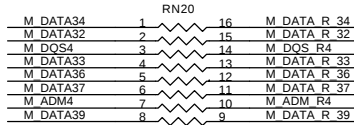
Title		
DDR SO-DIMM SKT		
Size	Document Number	Rev
A3	EGRET	SC
Date: Friday, July 23, 2004		
Sheet 8 of 50		

SERIES DAMPING

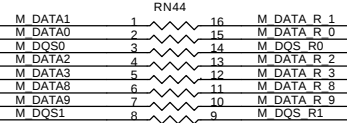
PLACE RNs CLOSE TO FIRST DM (DM1), < 0.75"
STRICT EQUAL LENGTH LIMITATION WITH DQS,
CB PINS



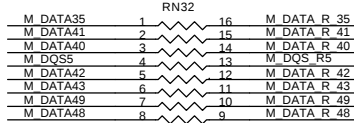
SRN10J-3



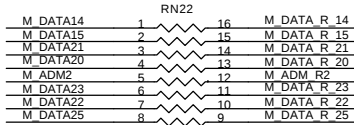
SRN10J-3



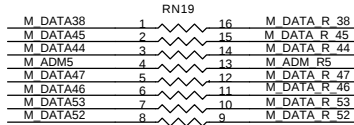
SRN10J-3



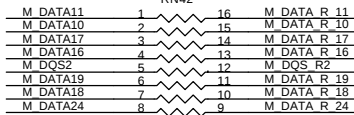
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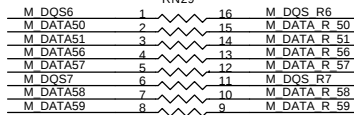
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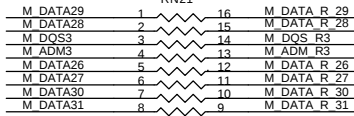
SRN10J-3



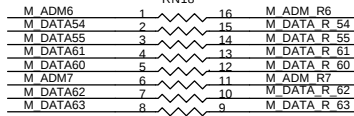
SRN10J-3



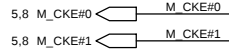
SRN10J-3



SRN10J-3



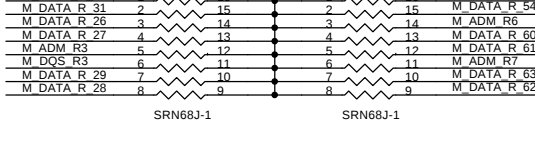
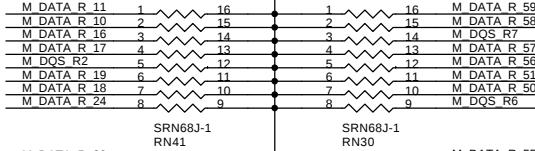
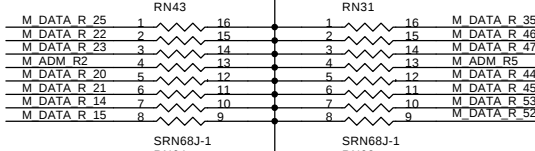
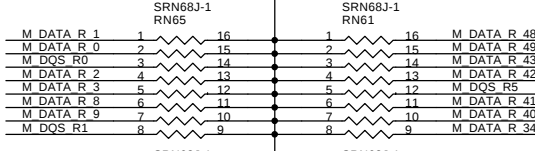
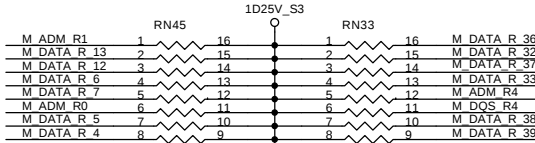
SRN10J-3



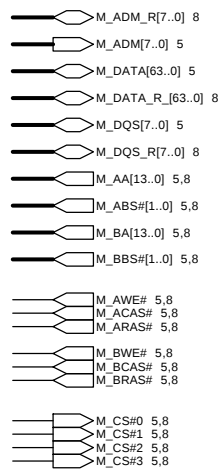
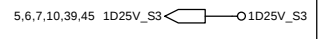
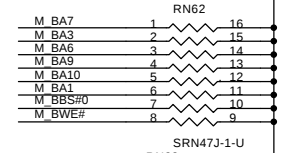
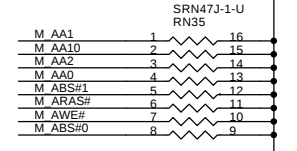
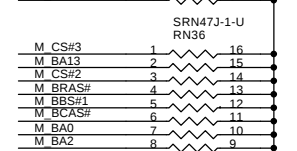
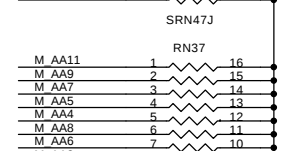
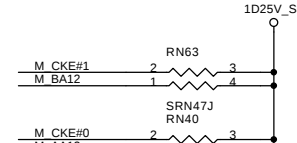
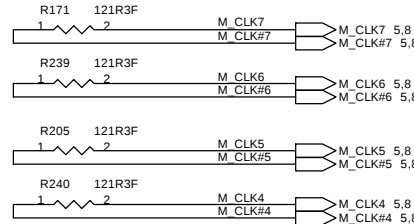
05/10
Remove the damping resistor for AMD suggest.

PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO SECOND DM (DM2)
NO EQUAL LENGTH LIMITATION



PLACE BETWEEN DM1, DM2
CLOSE TO FIRST DM (DM2) < 0.2", TO SECOND DM (DM1) < 1.1"
EQUAL LENGTH LIMITATION WITH SCK/SCK#

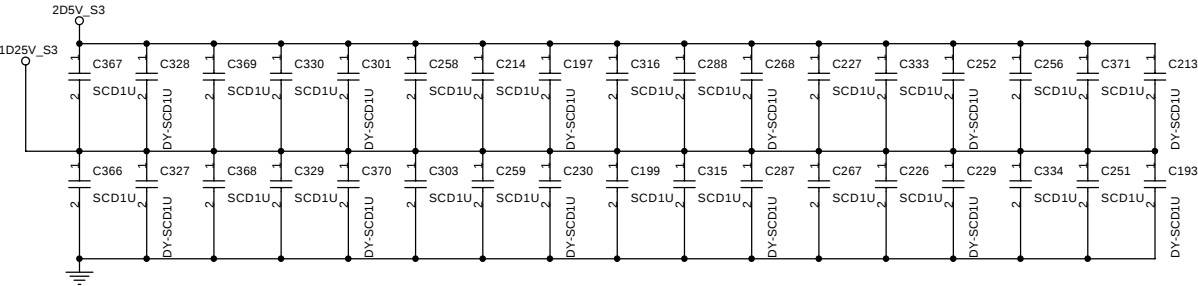
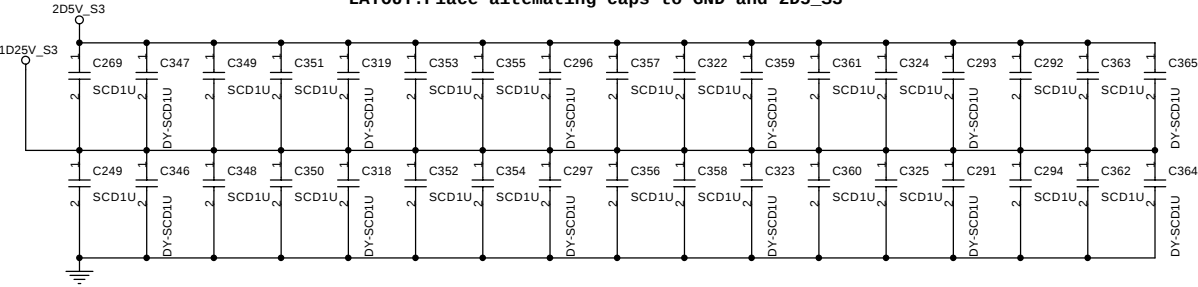


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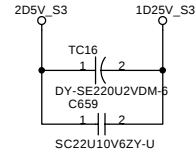
5,6,7,8,38,39,44,45,50 2D5V_S3

5,6,7,9,39,45 1D25V_S3

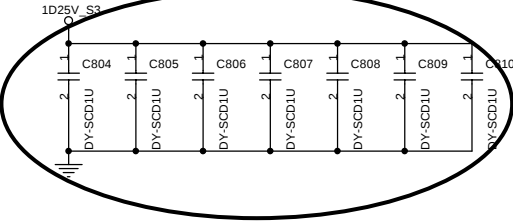
LAYOUT:Place altemating caps to GND and 2D5_S3



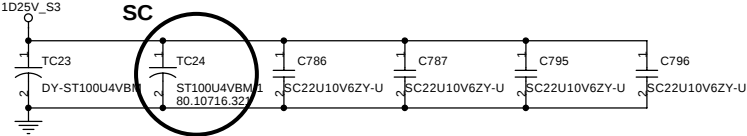
LAYOUT:Locate close to CPU socket.



SB

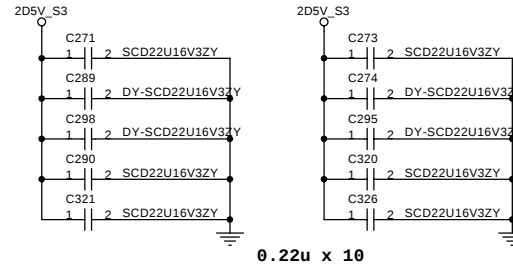


LAYOUT:Place at end of the DIMMs

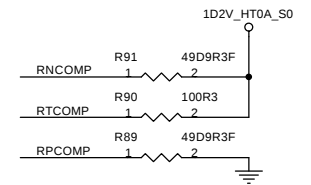
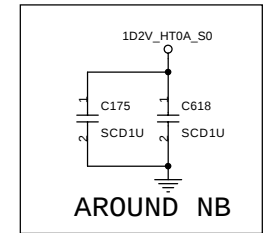
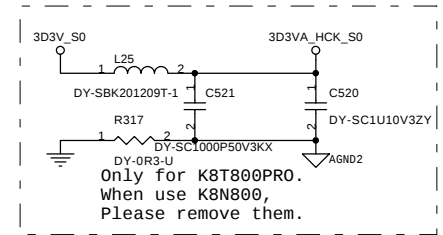
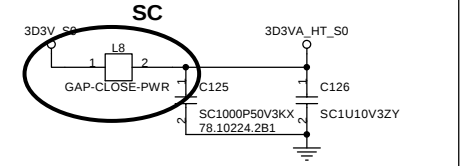
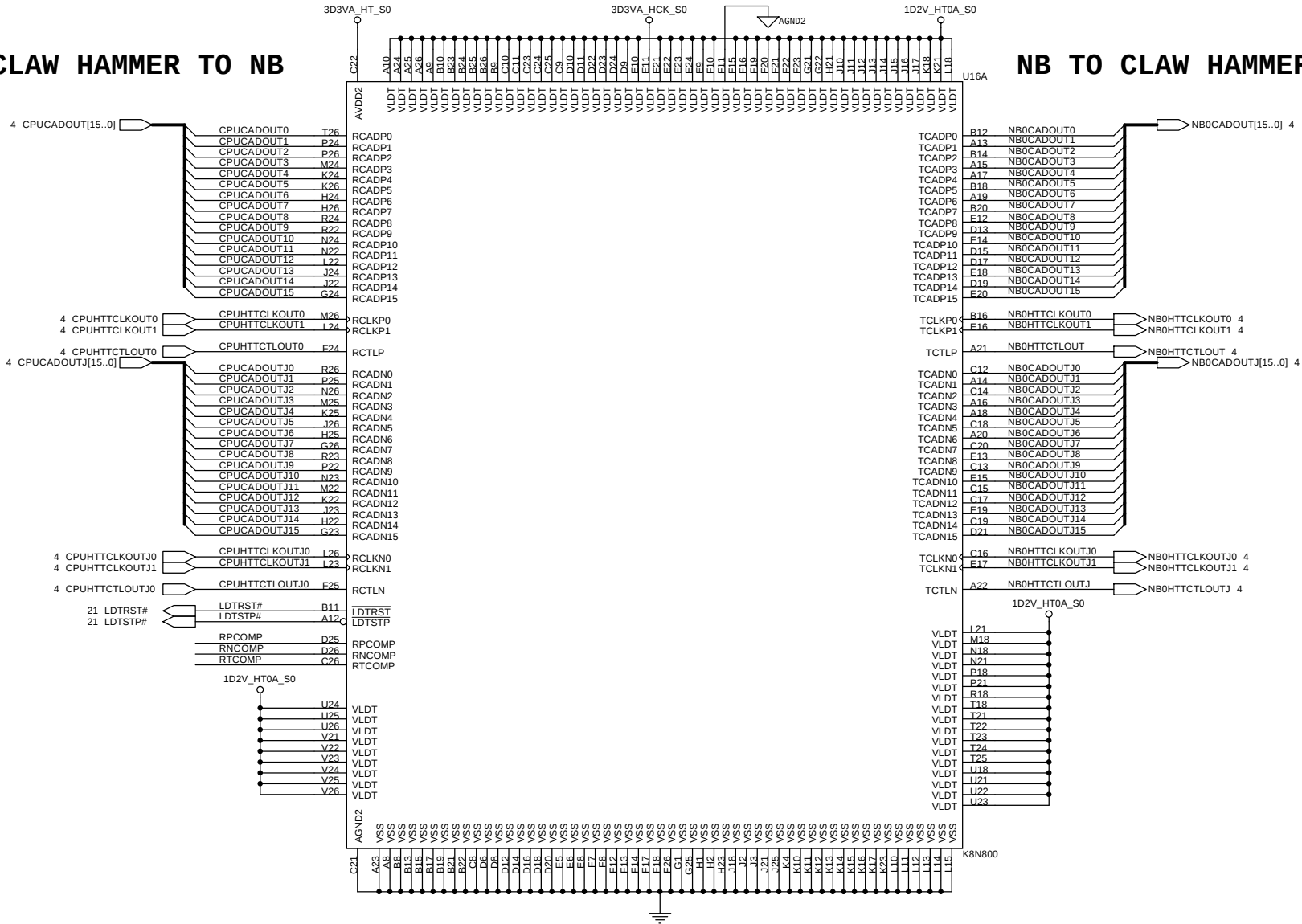


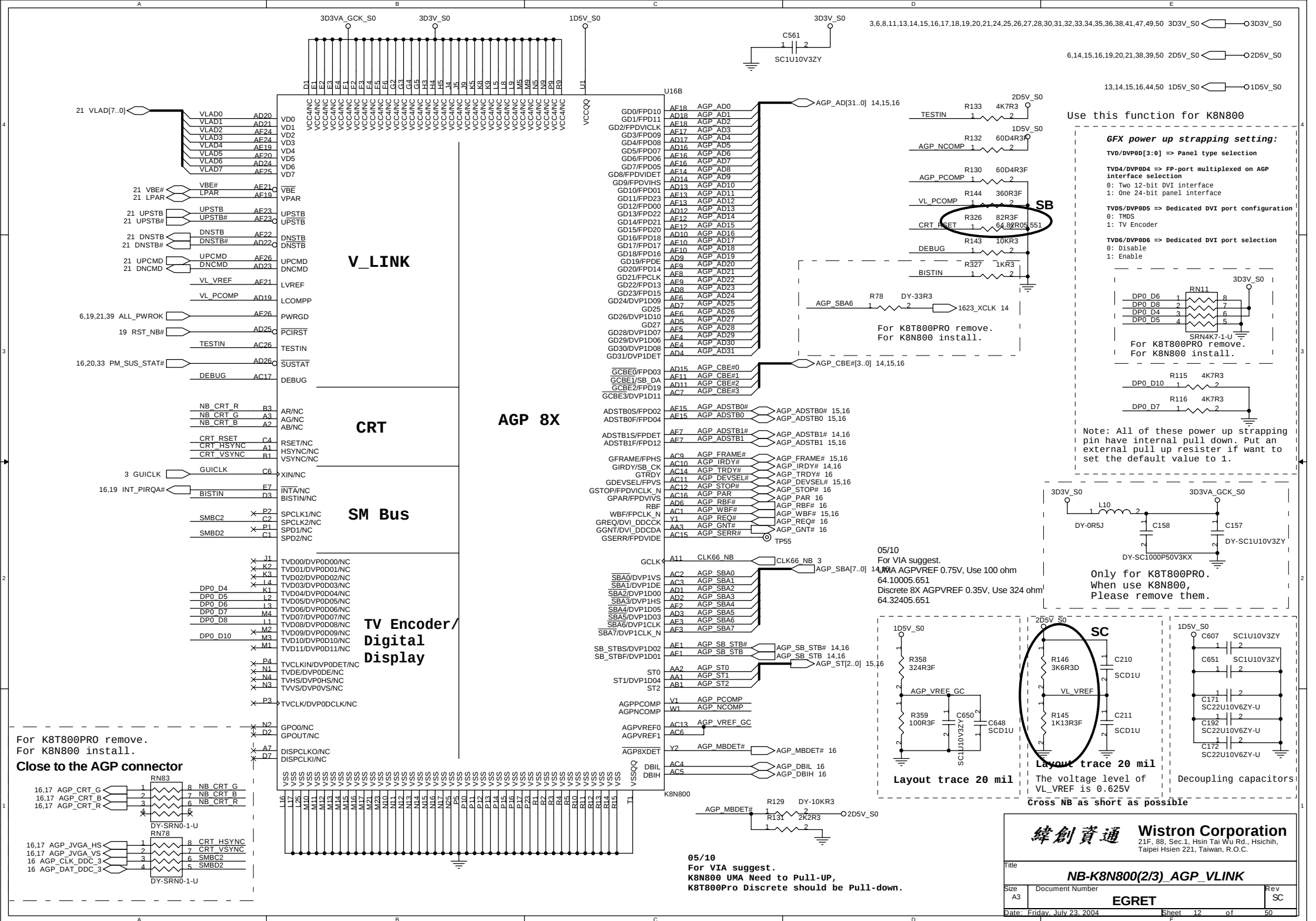
KEMET,NT:5.7, B2 size
ST100U4VBM-1 (80.10716.321)
Iripple=1.1A,ESR=70mohm
SANYO, NTS:6.1
Iripple=1.1A,ESR=70mohm
3.5/2.8/2.0
77.21071.031

LAYOUT:Place close to Power Pin of DDR socket.

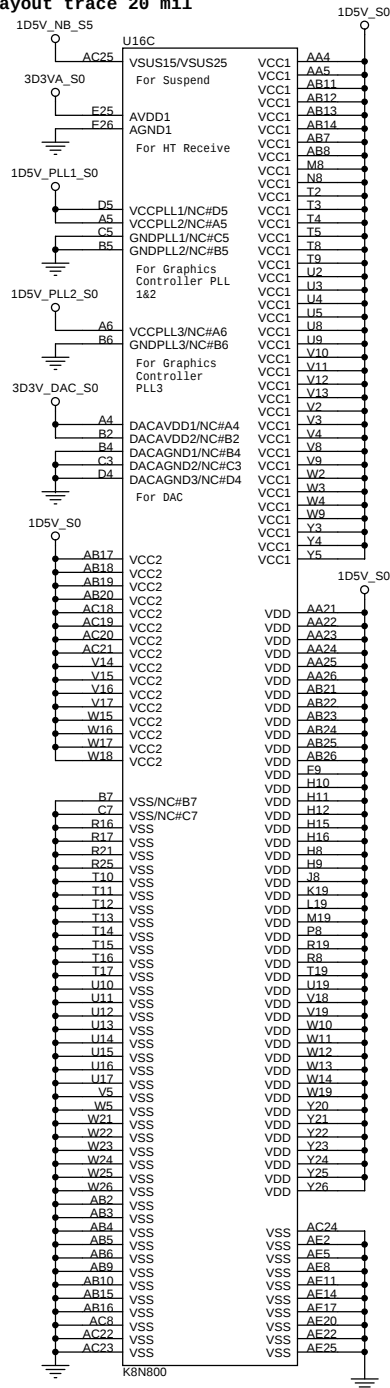


0.22u x 10

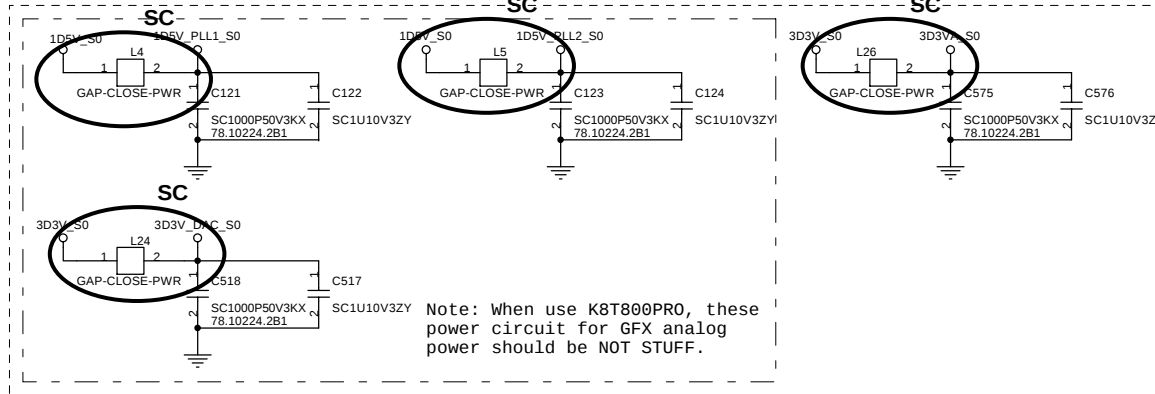




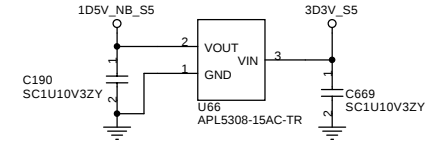
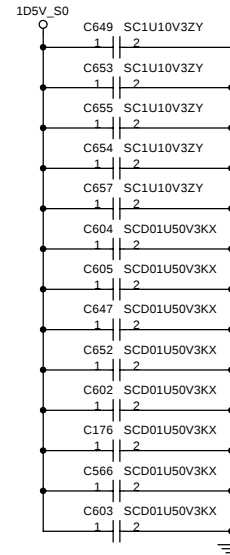
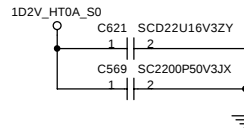
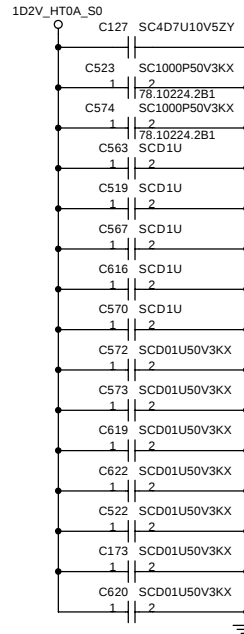
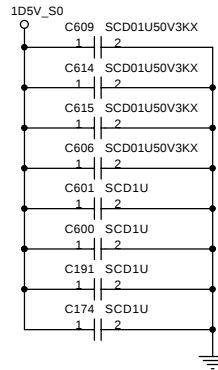
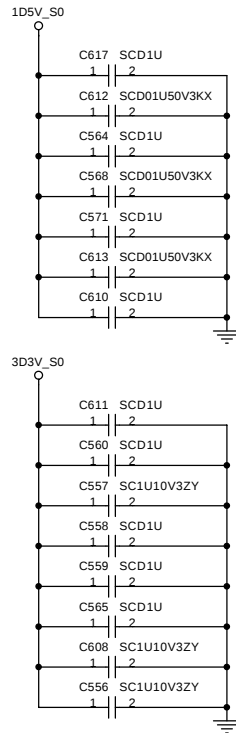
Layout trace 20 mil



Layout trace 20 mil

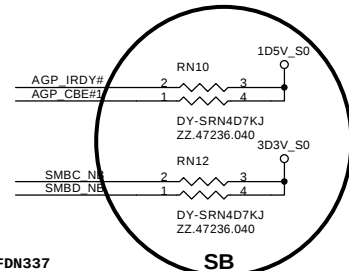
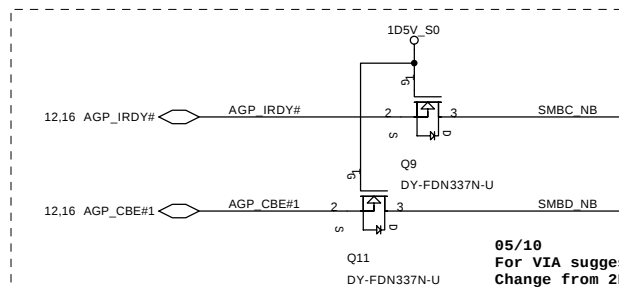
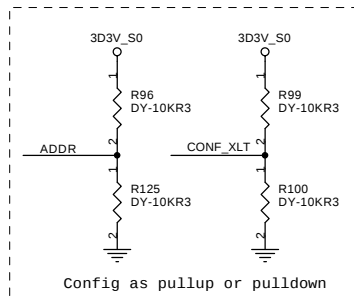
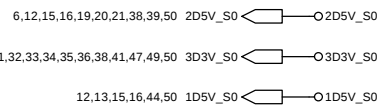
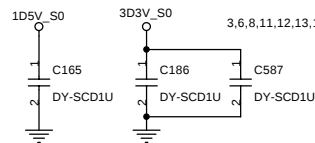
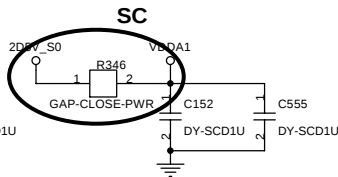
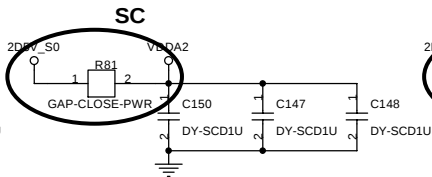
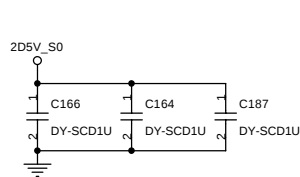


NEAR N/B ON BOT SIDE

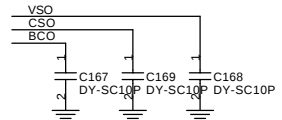
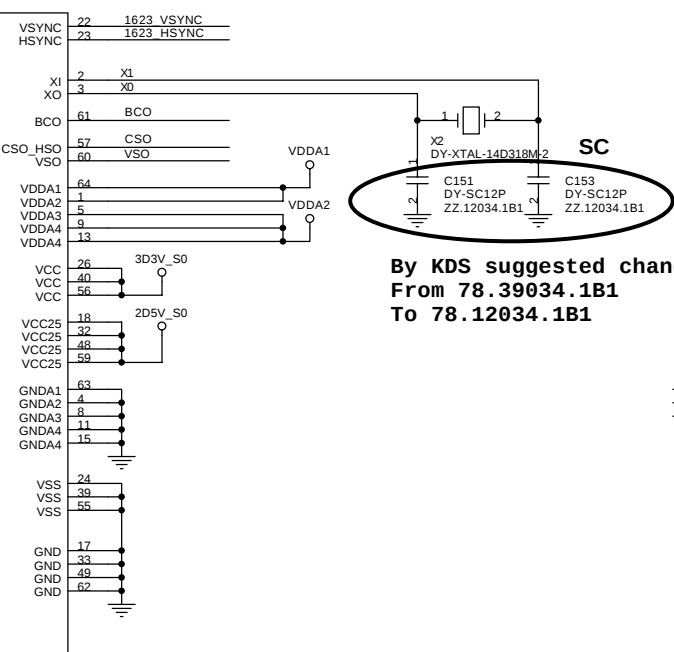
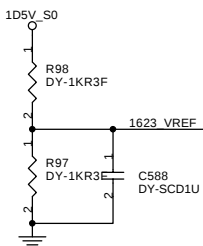
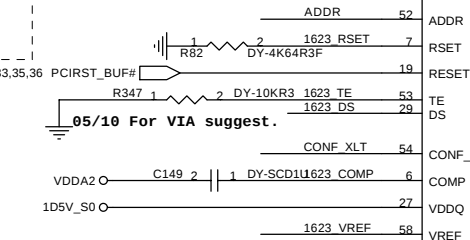
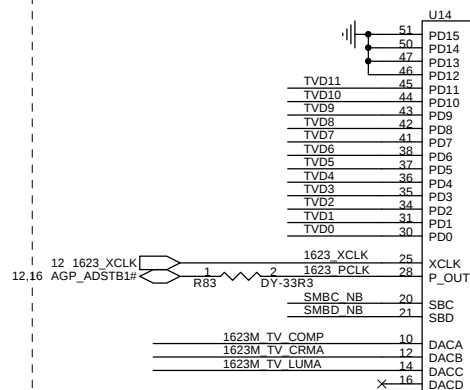
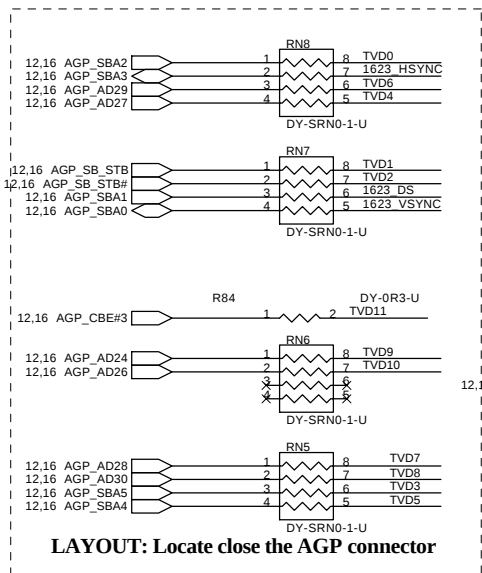


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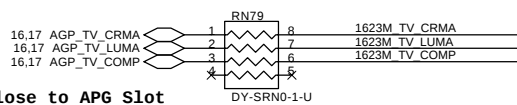
Title		
NB-K8N800(3/3) POWER		
Size A3	Document Number	Rev SC
EGRET		
Date: Friday, July 23, 2004	Sheet 13	of 50

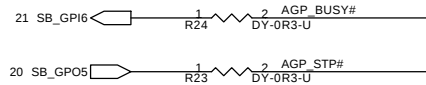
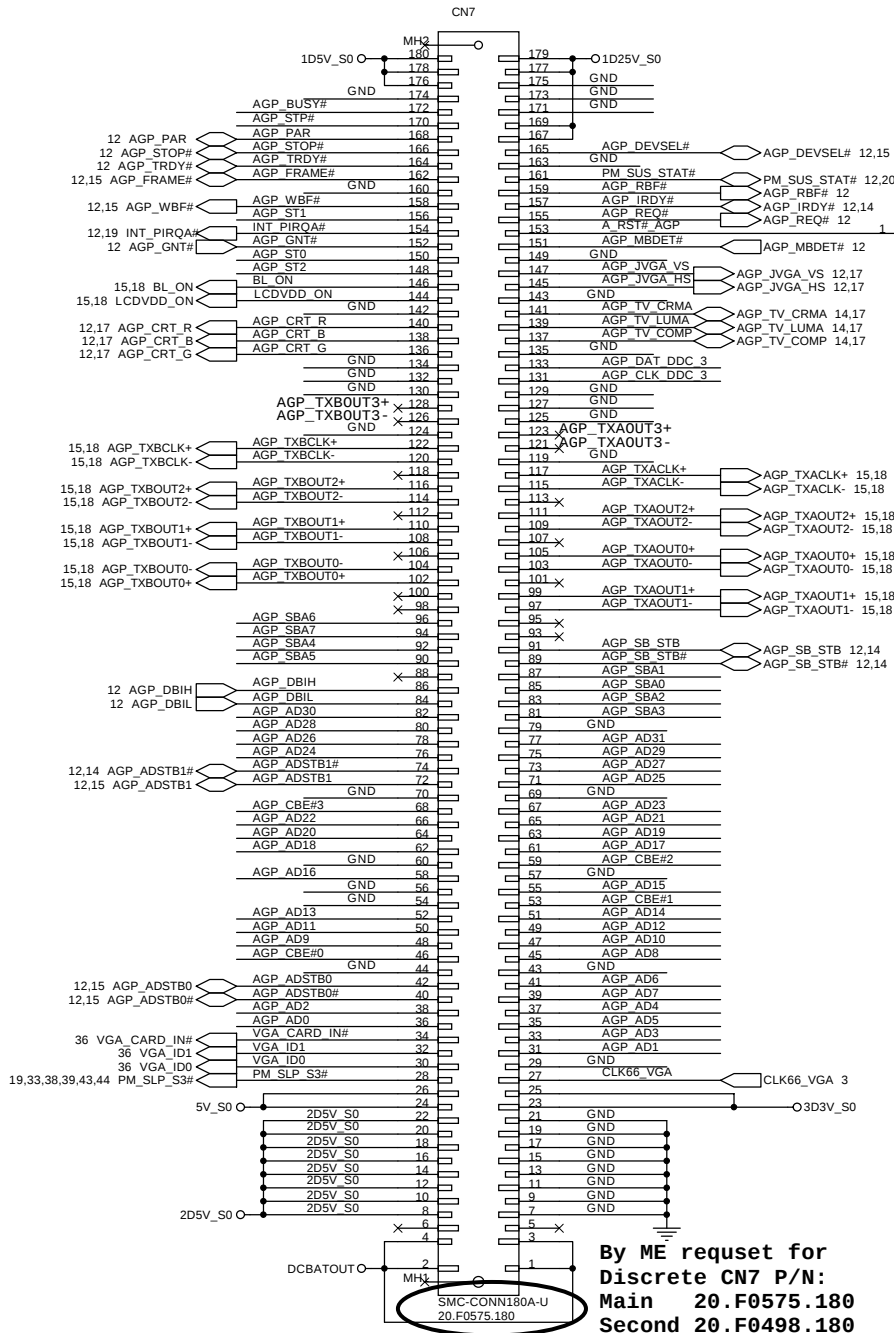


LAYOUT: Locate close the AGP connector

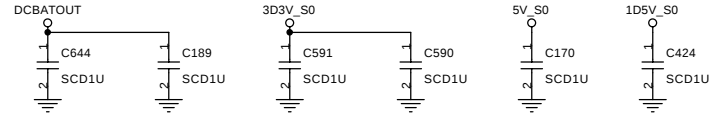
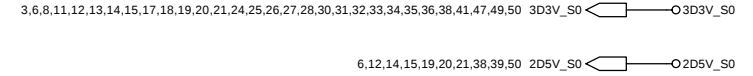


Note: Only for K8N800.
When use K8T800PRO,
Please remove them.

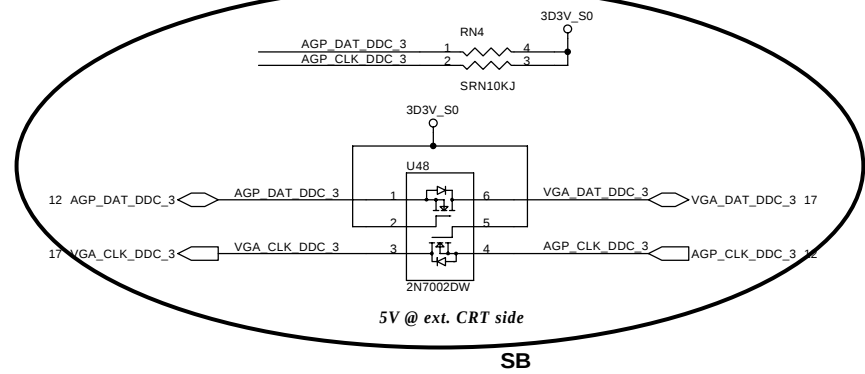




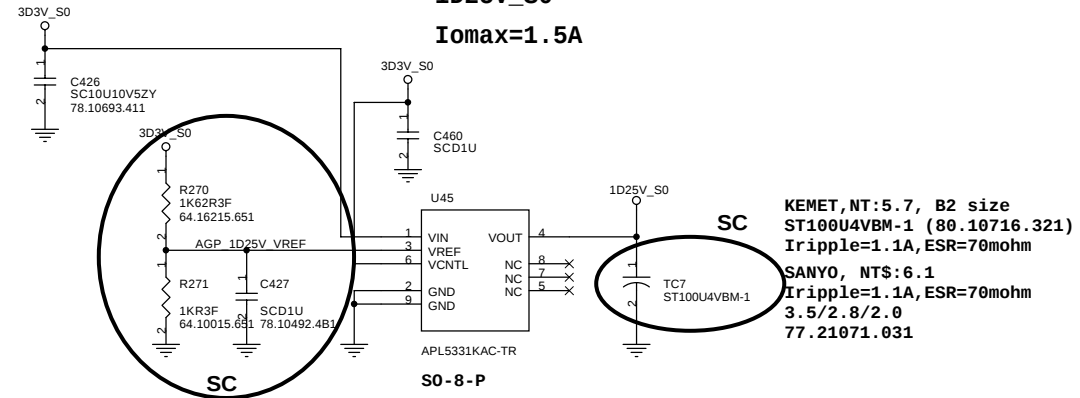
Debug only do not stuff



DDC_CLK & DATA level shift



1D25V_S0 Iomax=1.5A

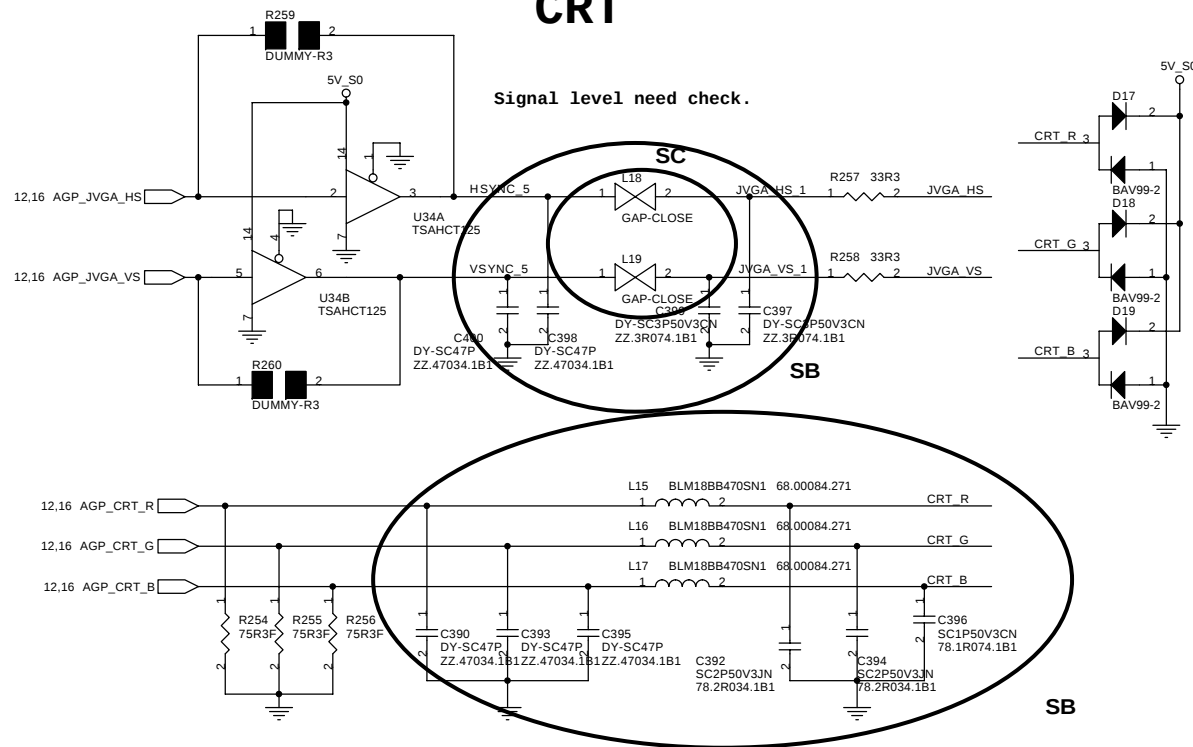


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Title			Graphic Conn.	
Size	Document Number	EGRET		Rev
A3				SC
Date: Friday, July 23, 2004		Sheet	16	of 50

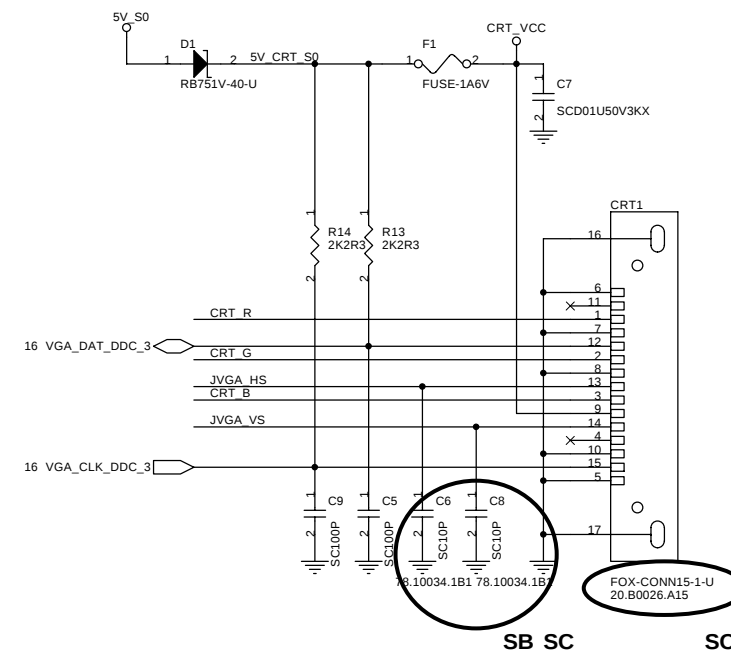
CRT

Signal level need check.



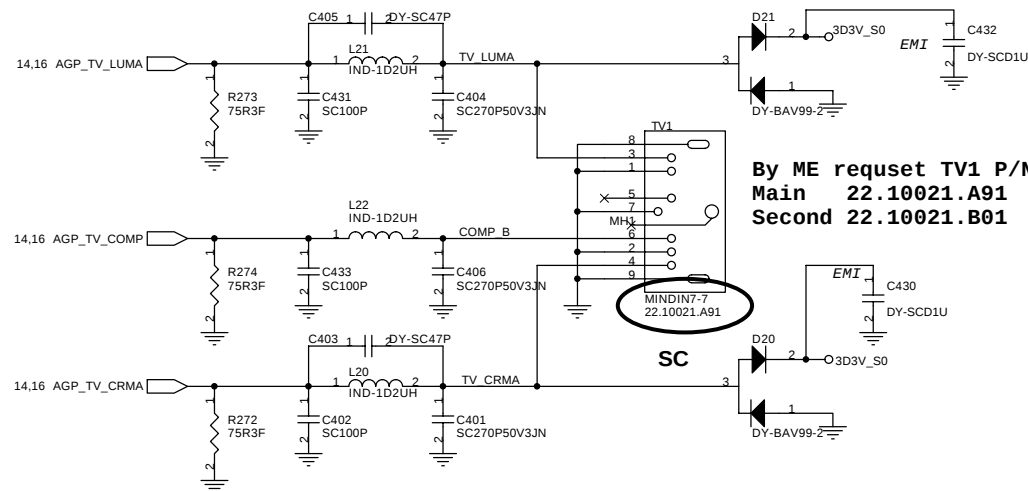
CRT CONN

200mA Rating/Spec 500mA

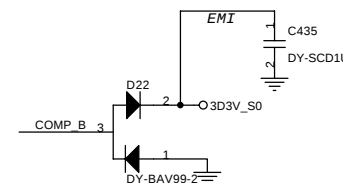


By ME request CRT1 P/N:
Main 20.B0026.A15
Second 20.B0034.015

TV CONN

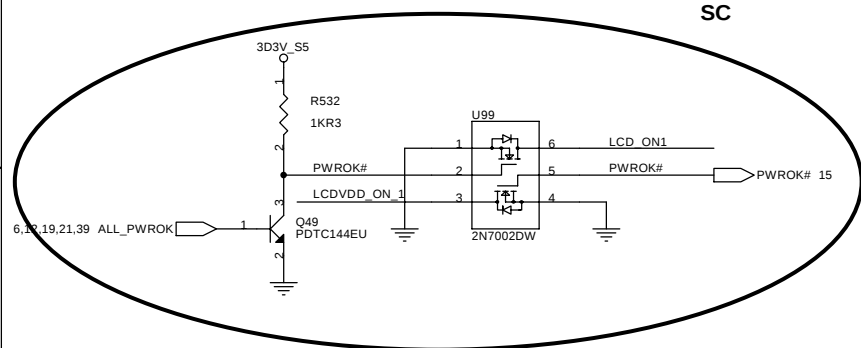
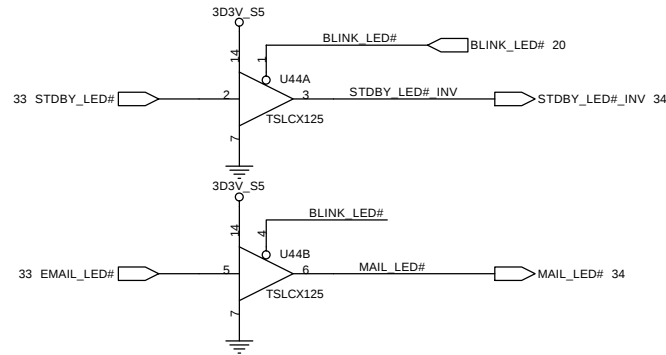
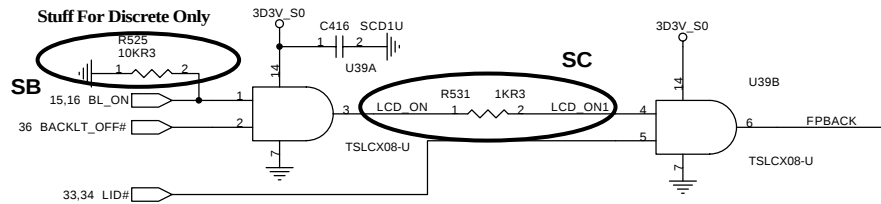


By ME request TV1 P/N:
Main 22.10021.A91
Second 22.10021.B01



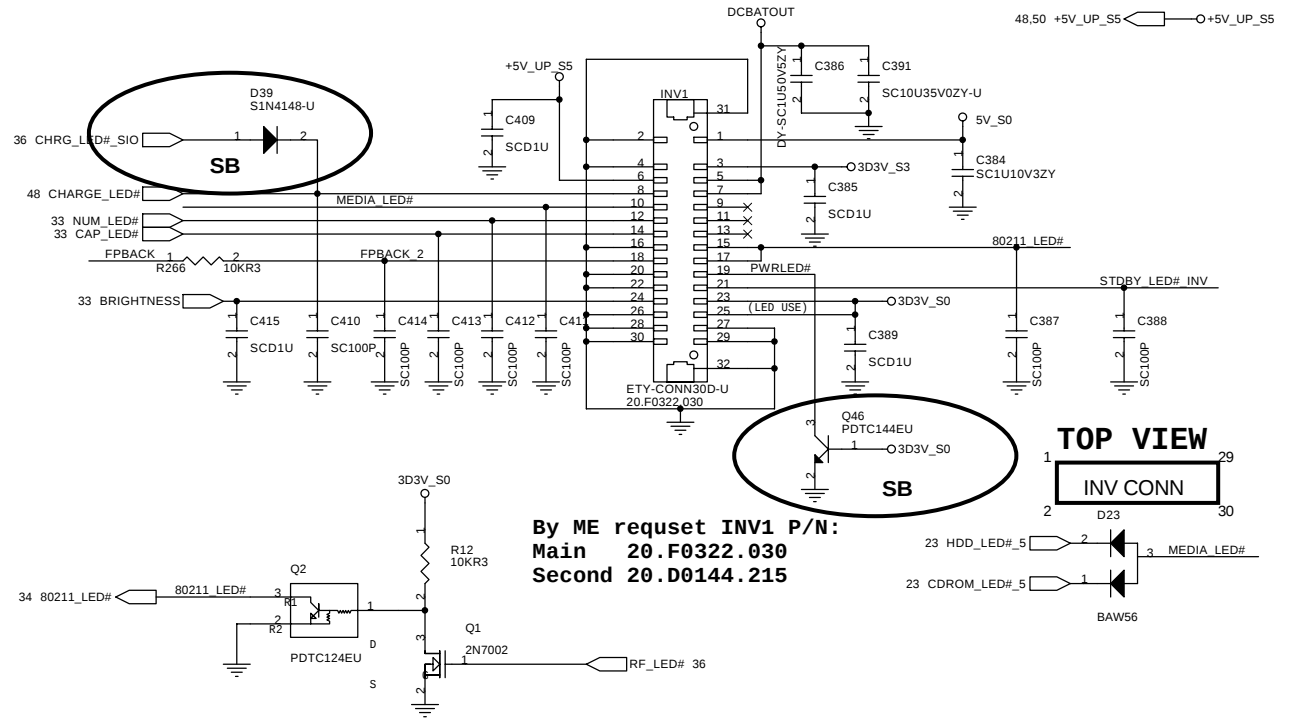
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Title			CRT / TV
Size	Document Number	Rev	
A3	EGRET	SC	
Date:	Friday, July 23, 2004	Sheet	17 of 50



INVERTER/LED

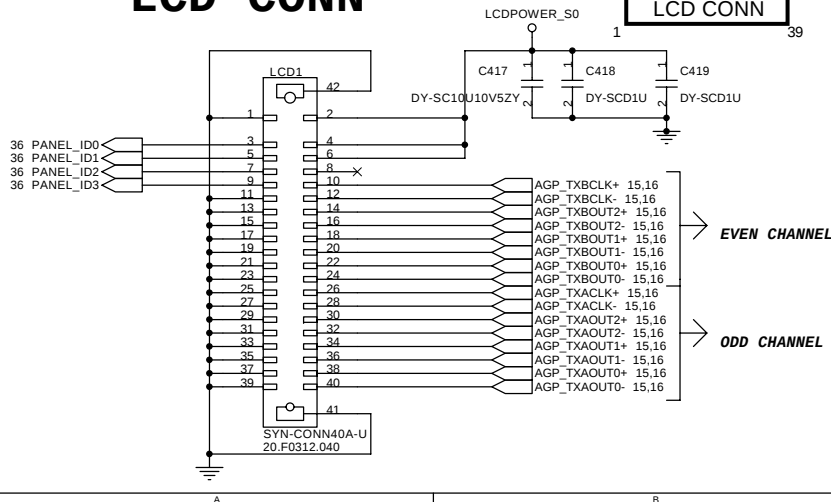
Layout trace 20 mil



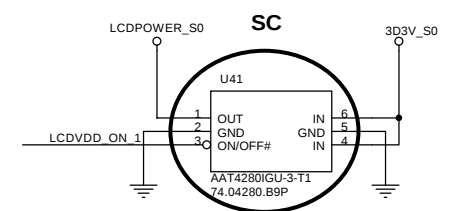
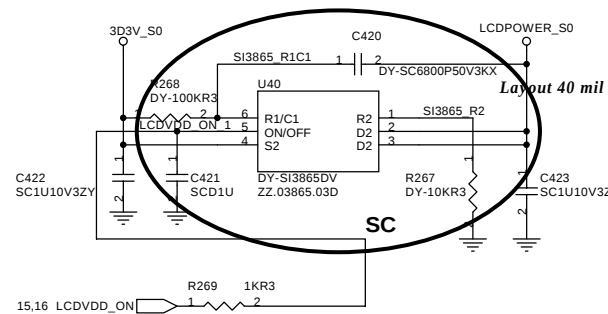
LCD CONN

TOP VIEW

LCD CONN

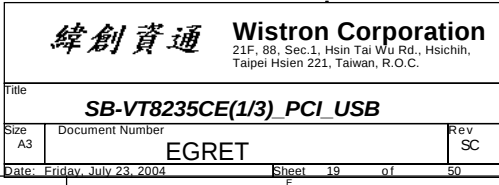


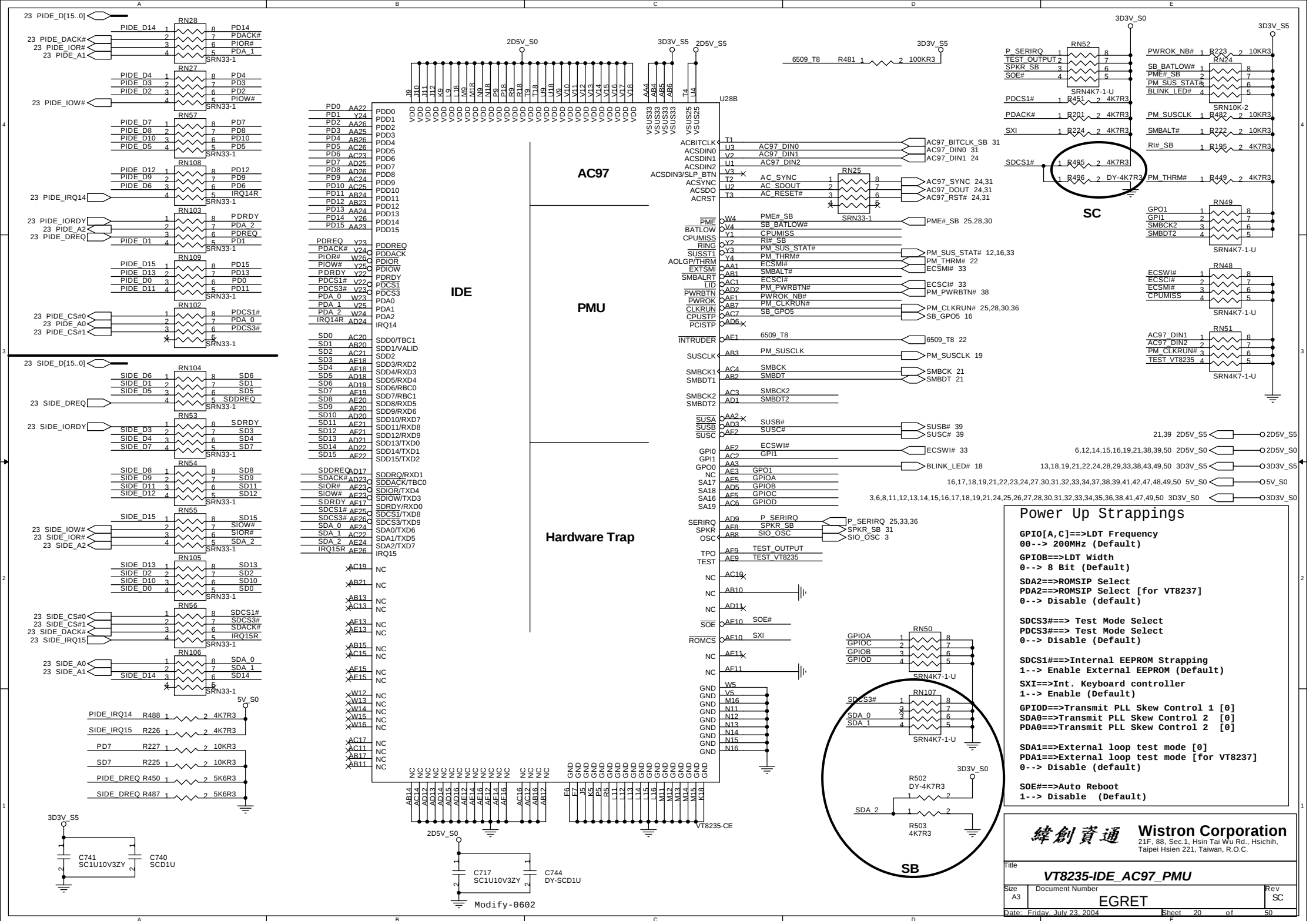
LCD POWER

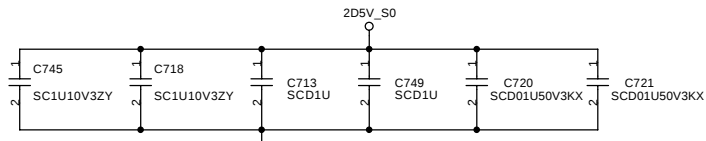


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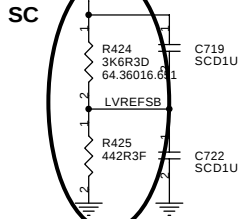
Title		
INV / LCD		
Size A3	Document Number	Rev SC
EGRET		
Date: Friday, July 23, 2004	Sheet 18 of 50	





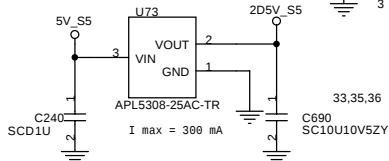


Layout trace 20 mil

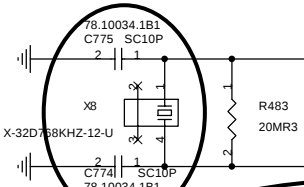


The voltage level of VL_VREF is 0.3V +/- 5%
Cross SB as short as possible

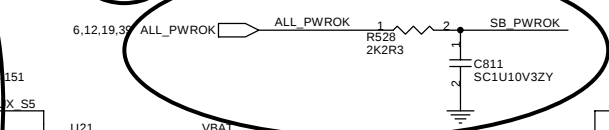
2D5V_S5



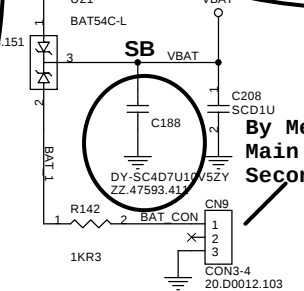
By KDS suggested change
From 12P to 10P
SC



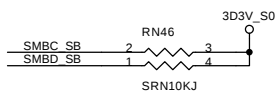
SC



SC



By Mechanism request CN9 P/N:
Main 20.D0012.103
Second 20.D0122.103

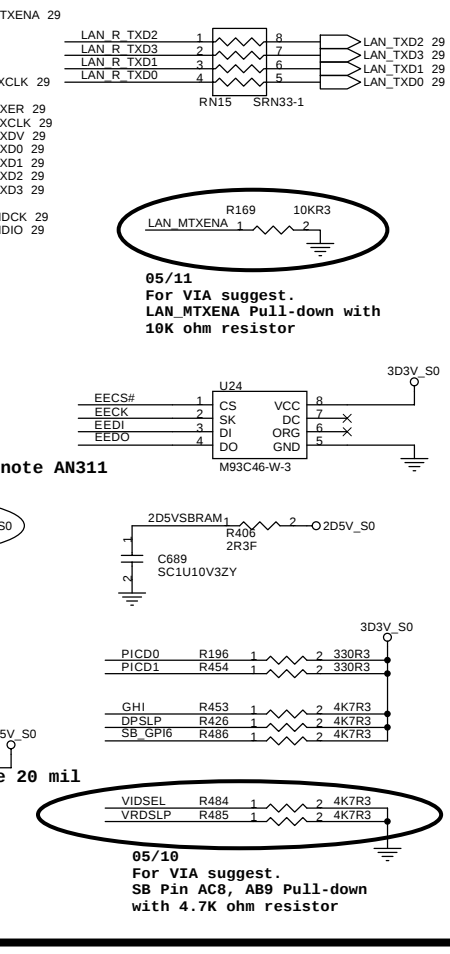
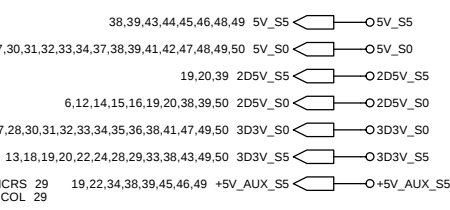
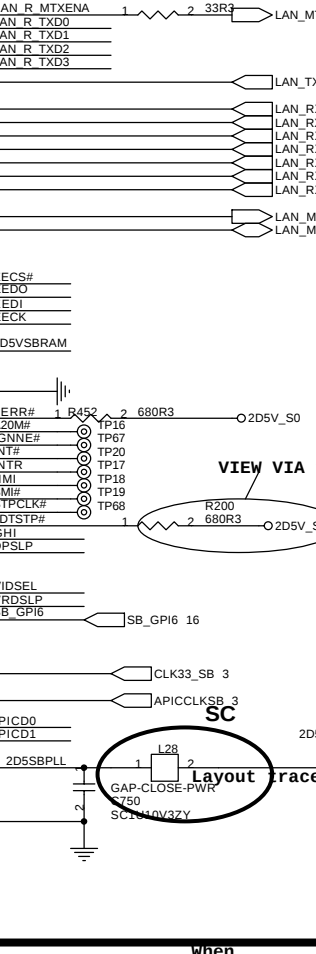
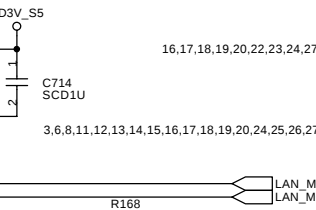
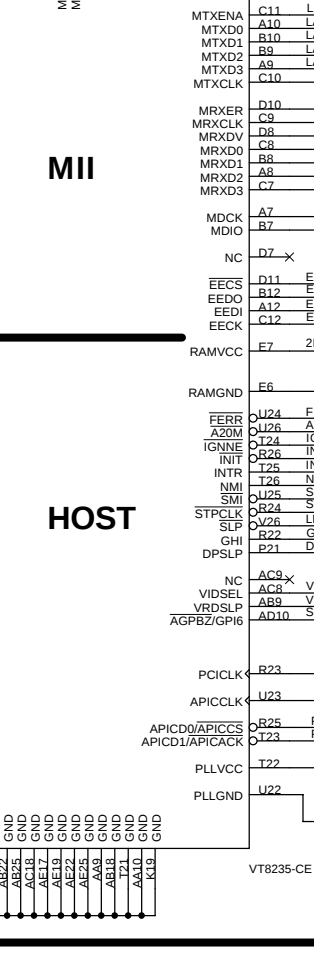
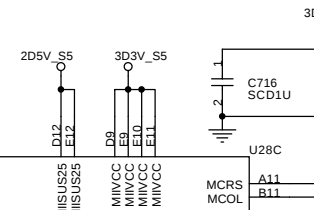
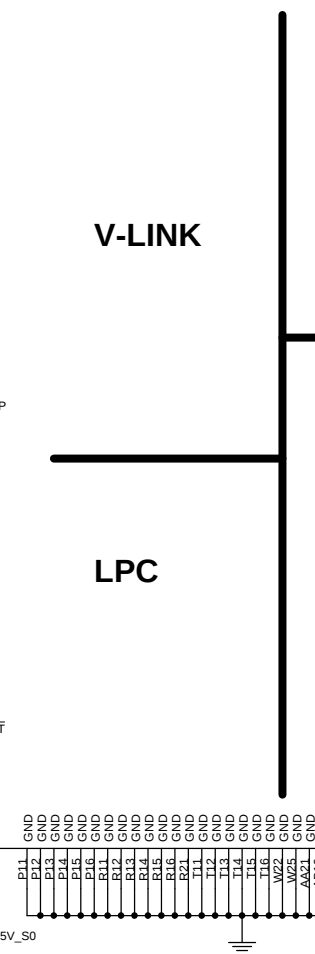
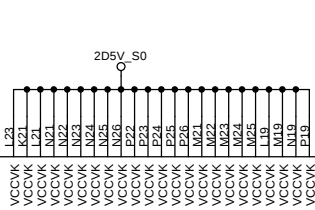


V-LINK

LPC

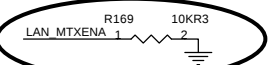
MII

HOST

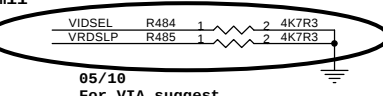
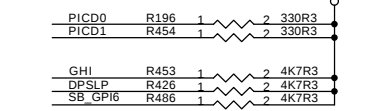
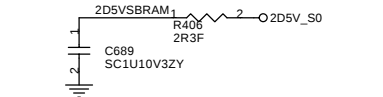
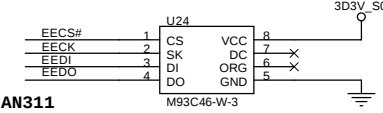


VIEW VIA note AN311

Layout trace 20 mil



05/11
For VIA suggest.
LAN_MTXENA Pull-down with
10K ohm resistor



05/10
For VIA suggest.
SB Pin AC8, AB9 Pull-down
with 4.7K ohm resistor

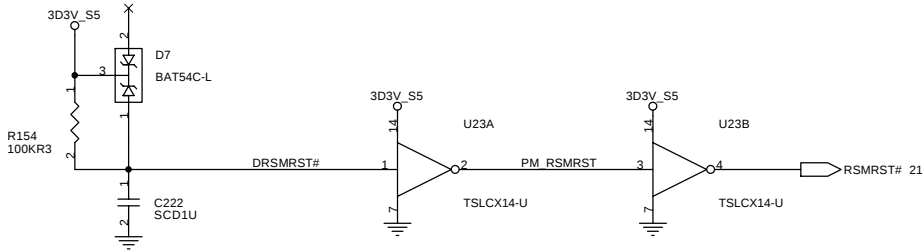
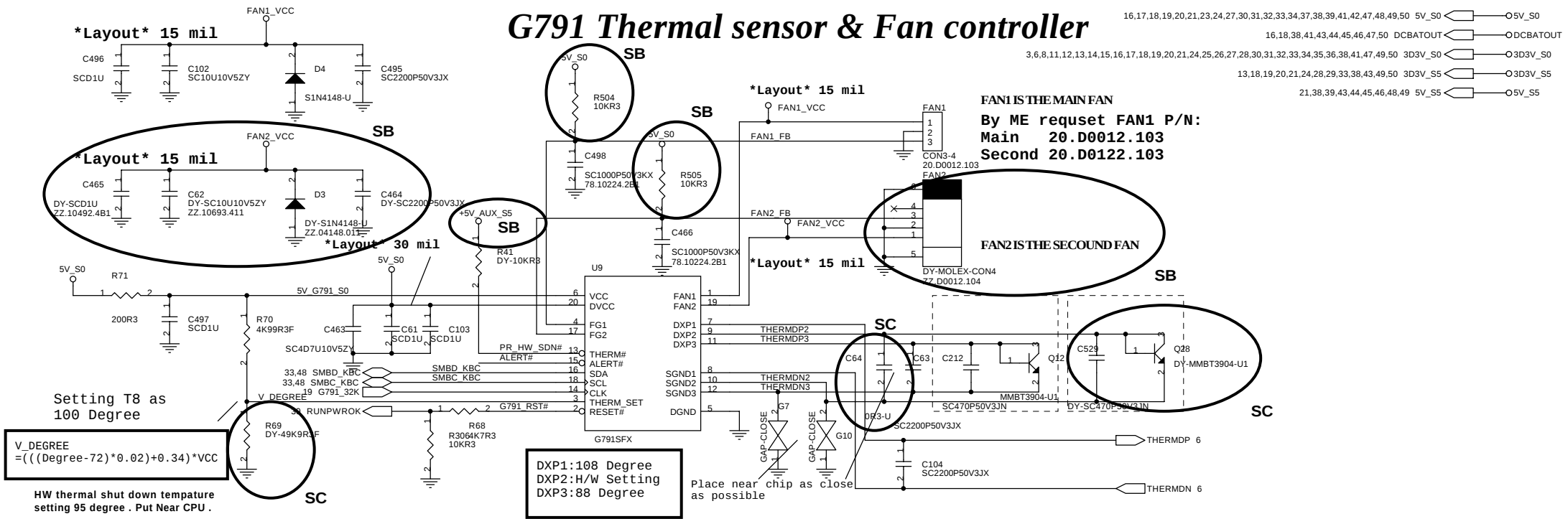
For K8N800 v.CD:
Not stuff R197
Stuff R198
For K8N800 v.CE:
Stuff R197
Not stuff R198

When
K8T800Pro : Remove
K8N800 : Install resistance

Reference VIA note AN311

When
K8T800Pro : Install resistance
K8N800 : Remove

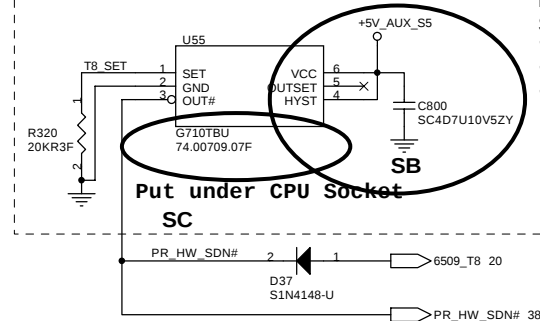
G791 Thermal sensor & Fan controller



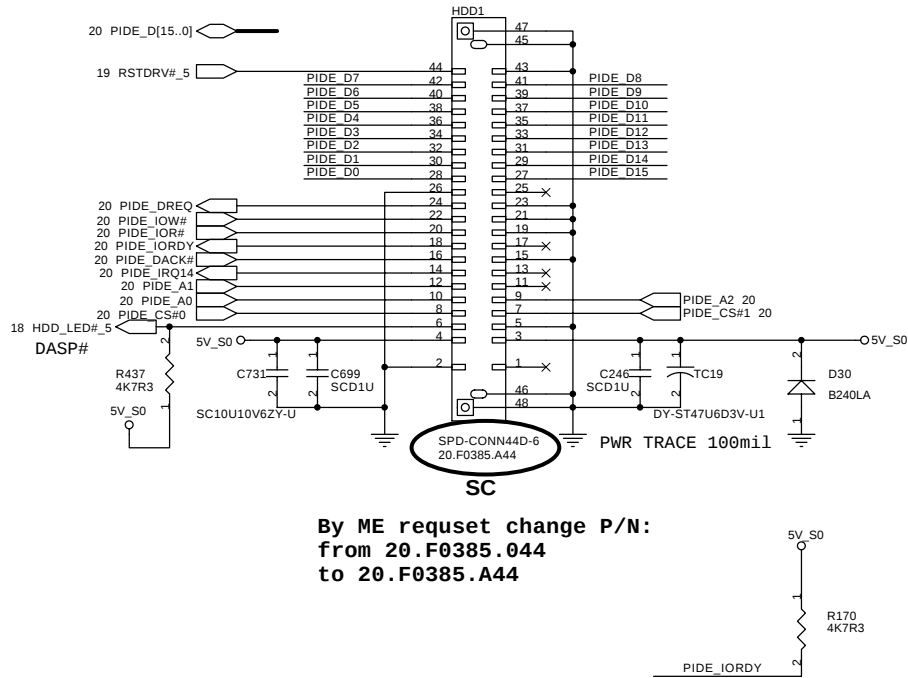
Dummy when G791 enhanced T8 function

T8_RSET:27K SET TO 80°C
 T8_RSET:20K SET TO 90°C
 T8_RSET:15K SET TO 100°C

By Sourcer request:
Main souce 74.00709.07F
Second souce
74.00710.03P
74.06509.07F
74.06510.A7P

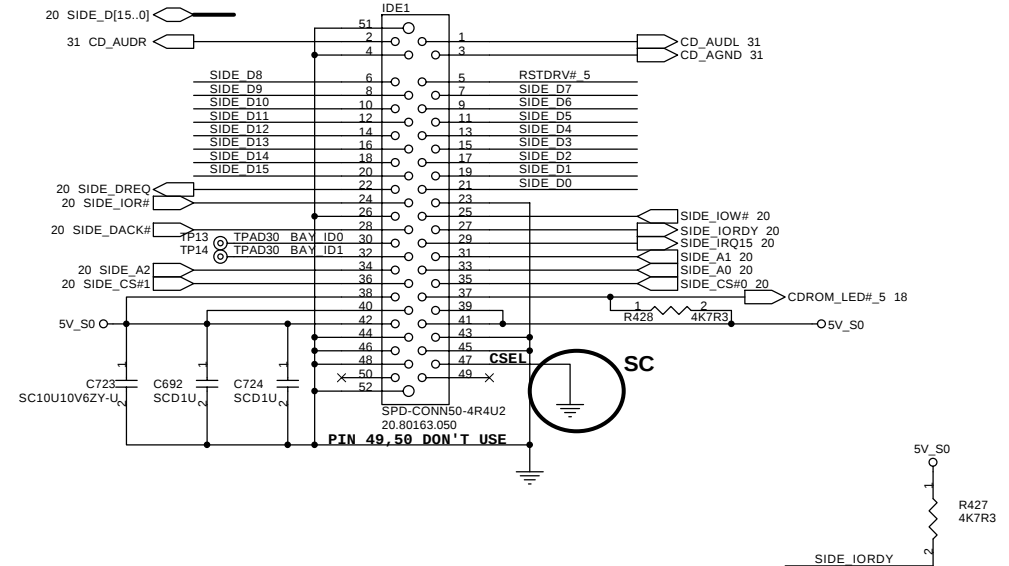


HDD



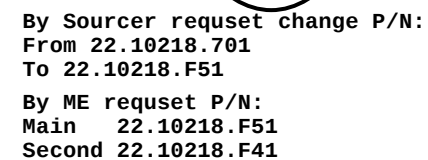
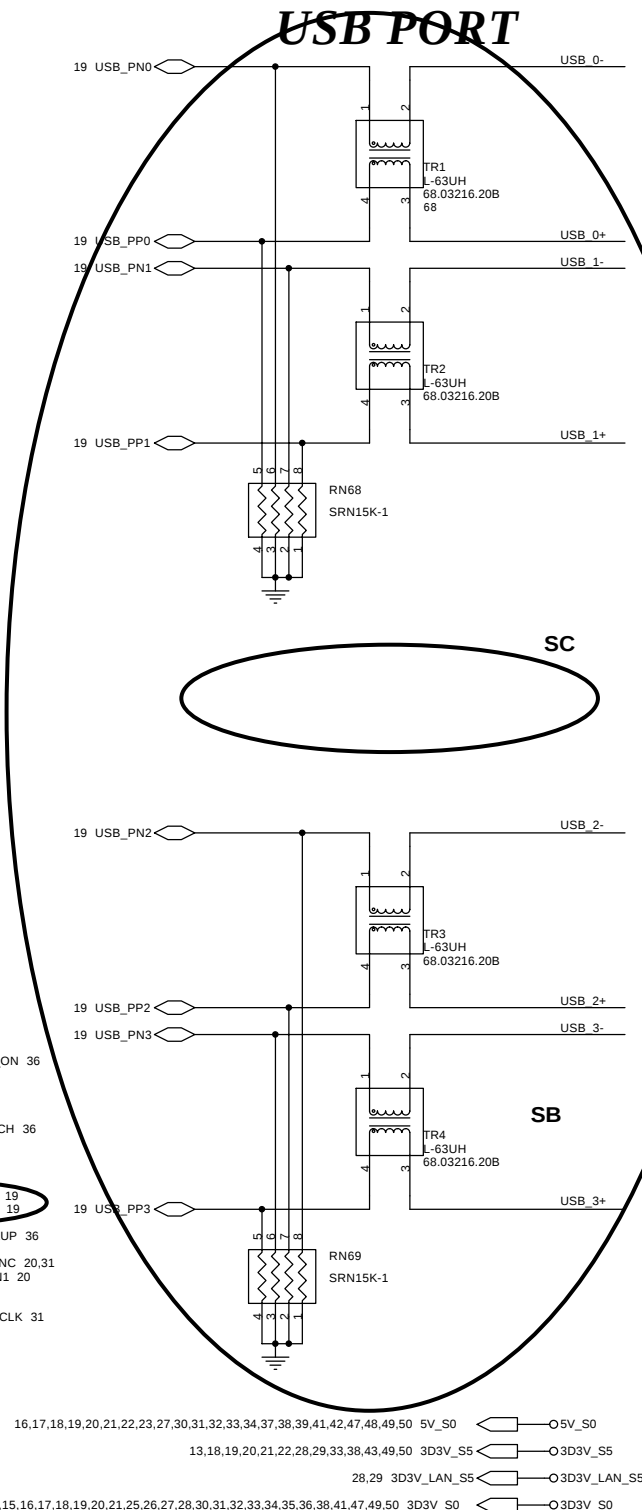
By ME request change P/N:
from 20.F0385.044
to 20.F0385.A44

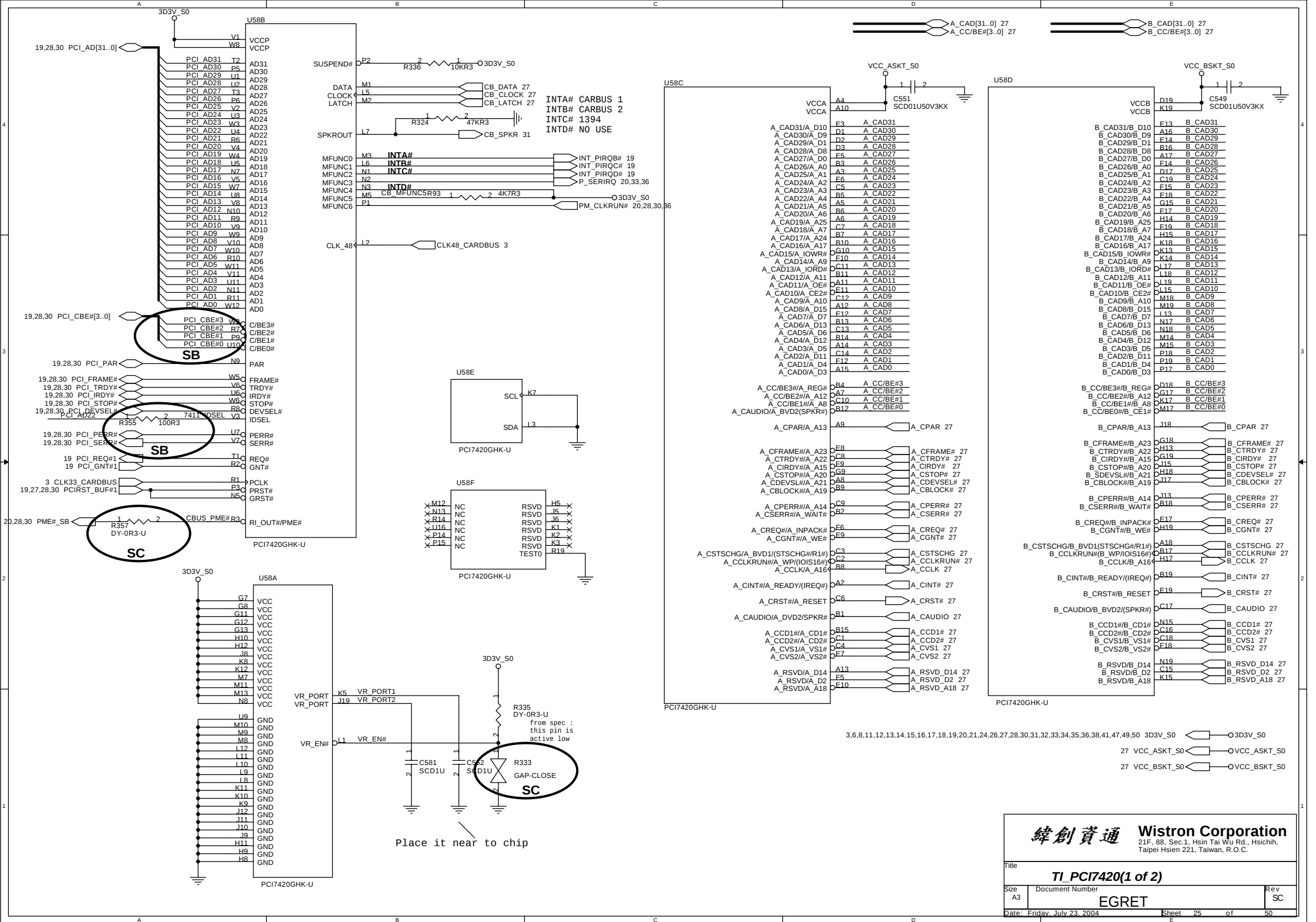
CDROM

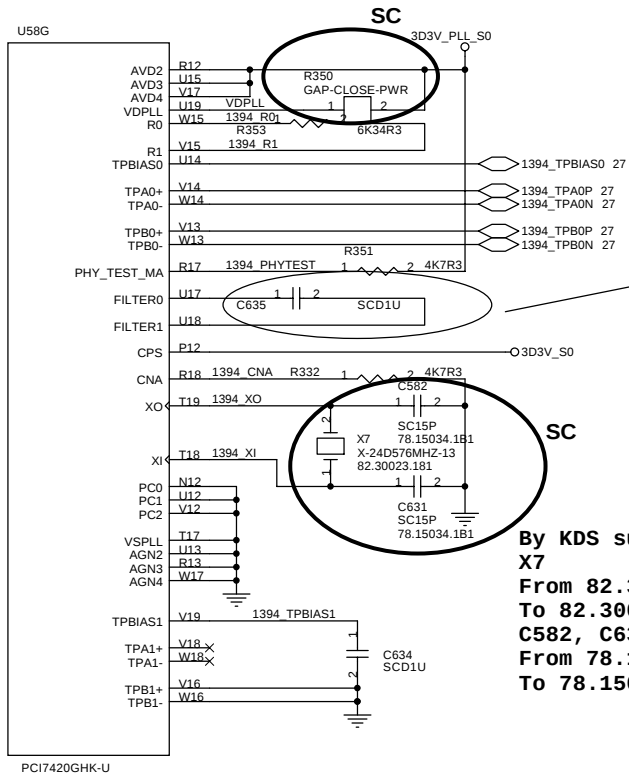


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		HDD / CDROM	
Size	Document Number	Rev	SC
A3	EGRET		
Date: Friday, July 23, 2004		Sheet	23 of 50

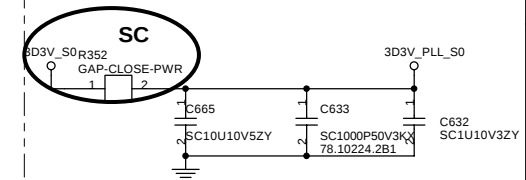
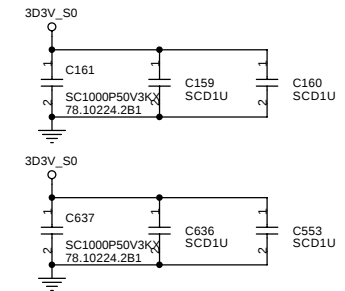
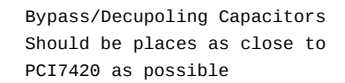
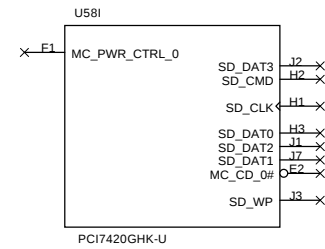
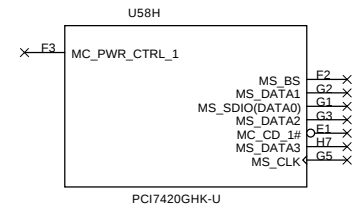


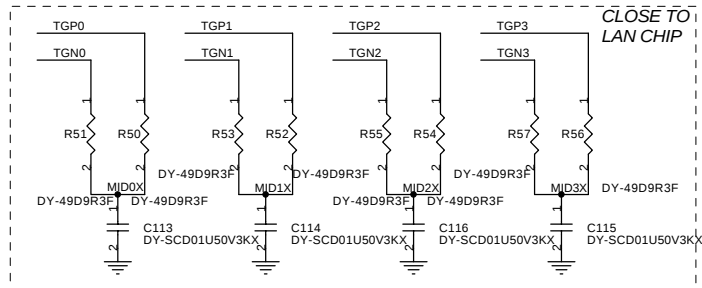




7420 SPEC Description

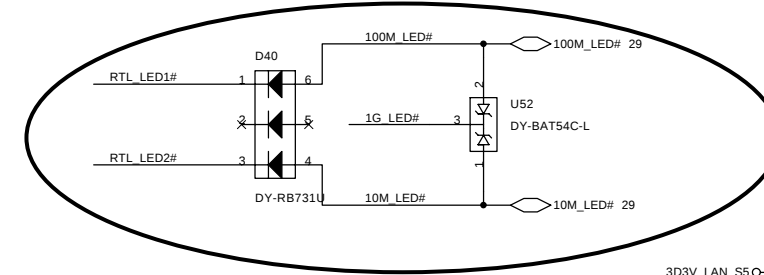
By KDS suggested change
X7
From 82.30023.161
To 82.30023.181
C582, C631
From 78.10034.1B1
To 78.15034.1B1



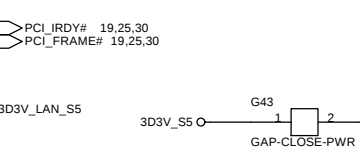
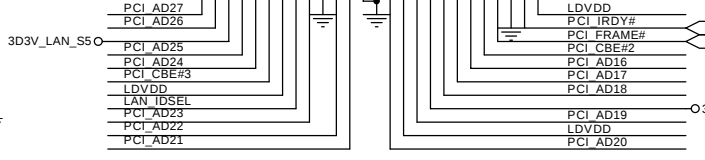
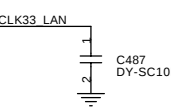
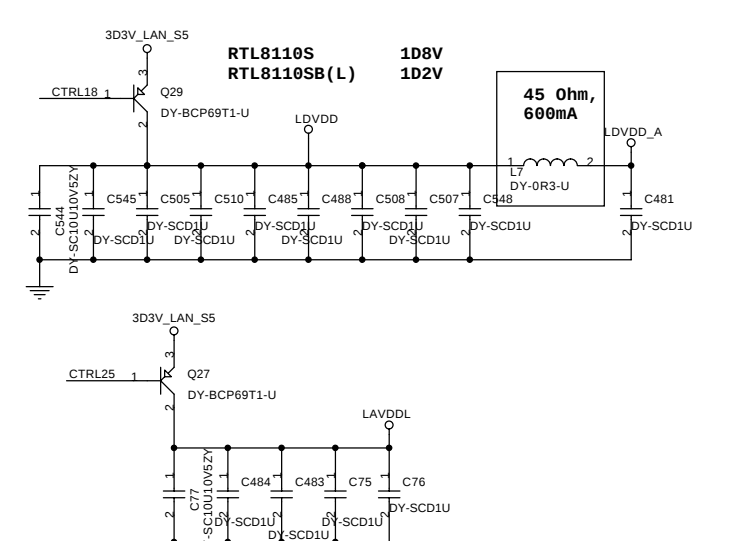
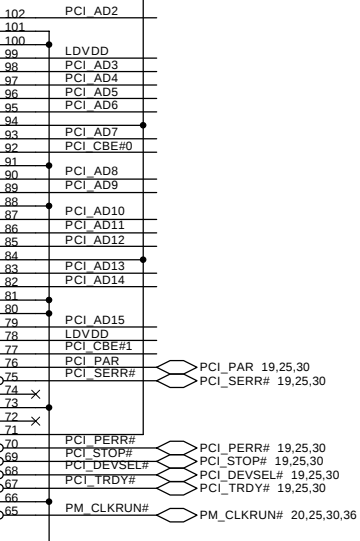
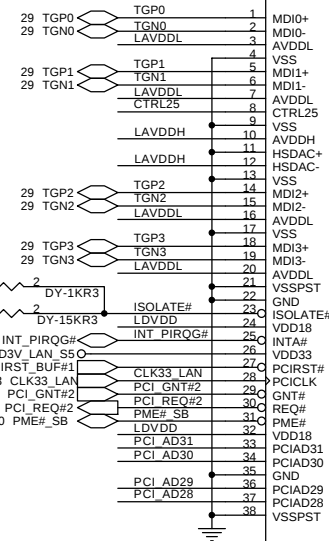
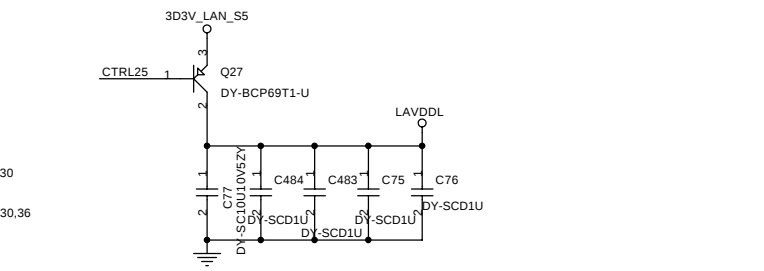
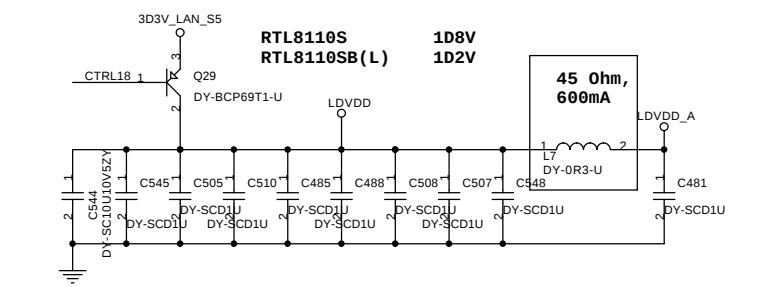
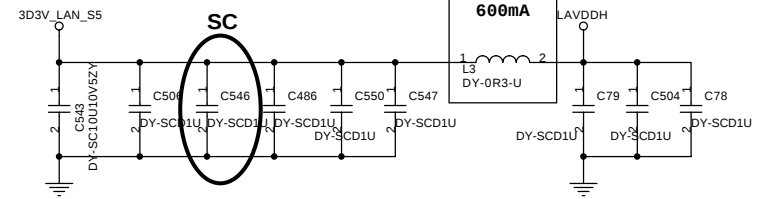
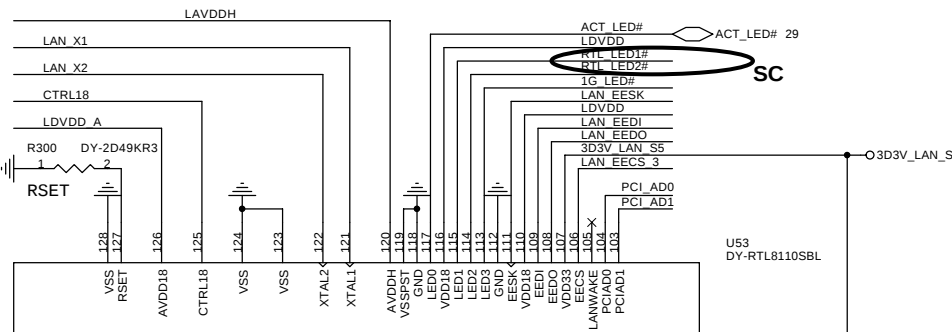
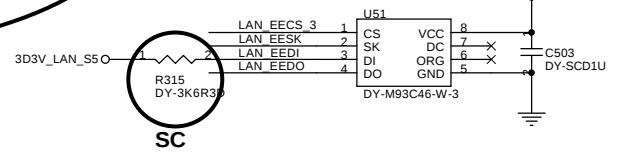
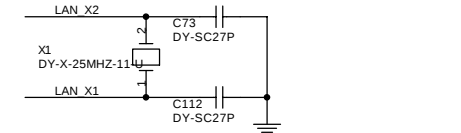


19,25,30 PCI_AD[31..0]
19,25,30 PCI_CBE#[3..0]

SC



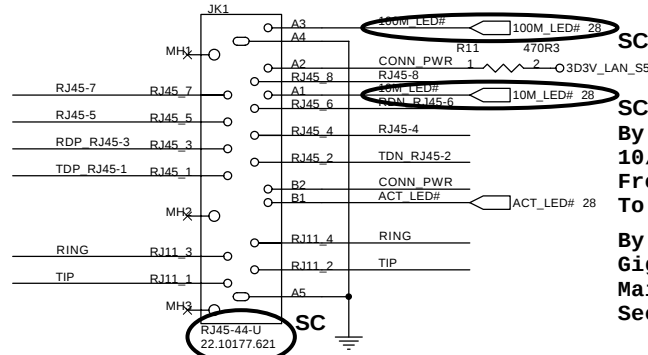
3,6,8,11,12,13,14,15,16,17,18,19,20,21,24,25,26,27,30,31,32,33,34,35,36,38,41,47,49,50 3D3V_S0
3D3V_S0
3D3V_LAN_S5
24,29 3D3V_LAN_S5



Form containing the title "LAN RTL8110SBL", the date "Friday, July 23, 2004", the sheet number "28 of 50", and the revision "SC".

Link: Green - 10Mbps/802.11b
 Orange - 100Mbps/802.11a
 Yellow - 1Gbps

Activity: Yellow

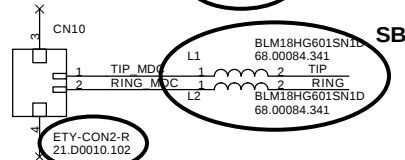


SC

SC

By ME request for
 10/100 LAN change P/N:
 From 22.10177.601
 To 22.10177.621

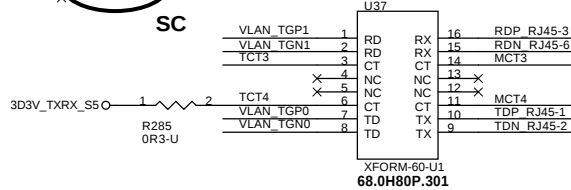
By ME request for
 GigaLAN JK1 P/N:
 Main 22.10177.601
 Second 22.10245.771



SB

By ME request change P/N:
 From 20.D0121.102
 To 21.D0010.102

SC



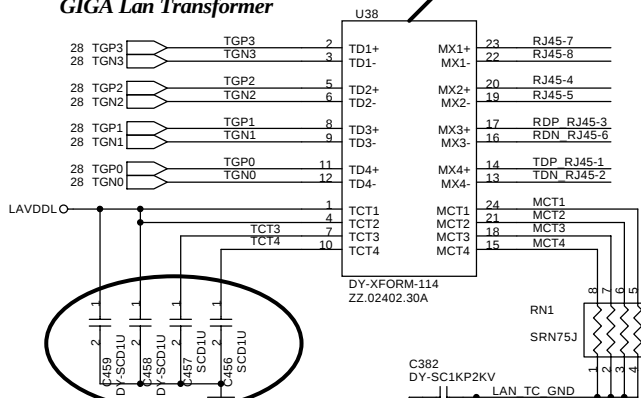
Stuff for VT6103L
 10/100M Lan Transformer

By Sourcer request change P/N:
 From 68.H0013.301
 To 68.0H80P.301

By Sourcer request change P/N:
 From 68.H5015.301
 To 68.02402.30A

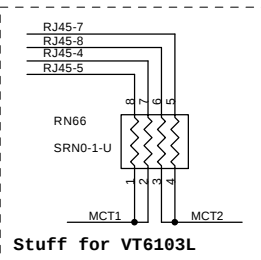
Stuff for RTL8110SBL

GIGA Lan Transformer

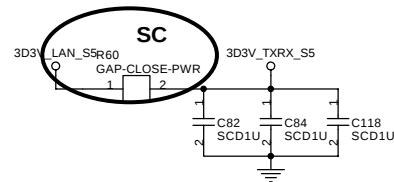


For GigaLAN Cap. change
 to SCD01U50V3KX
 78.10324.2B1

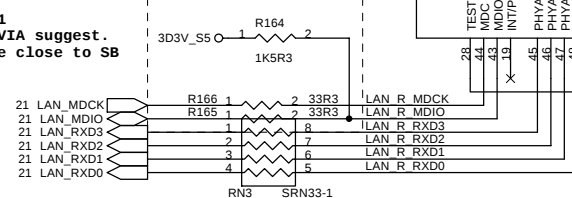
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.



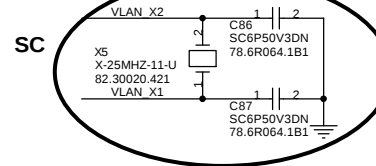
Stuff for VT6103L



05/11
 For VIA suggest.
 Place close to SB

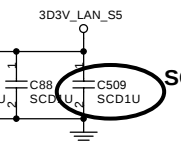


SC

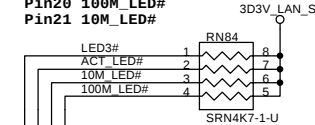


05/11
 For VIA suggest.
 Change from 18P to 22P

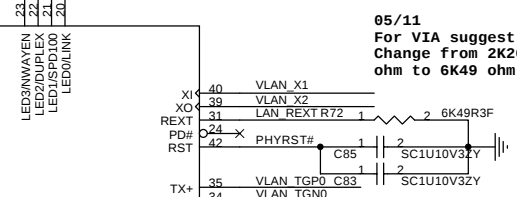
By KDS suggested change
 X5
 From 82.30020.161
 To 82.30023.421
 C86, C87
 From 22P To 6P



05/11
 For VIA suggest.
 Pin20 100M_LED#
 Pin21 10M_LED#

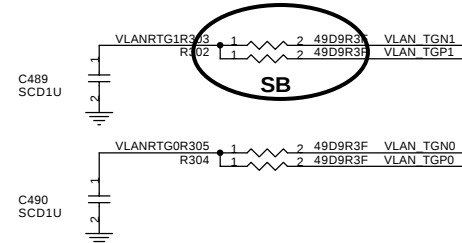


05/11
 For VIA suggest.
 Change from 2K26
 ohm to 6K49 ohm

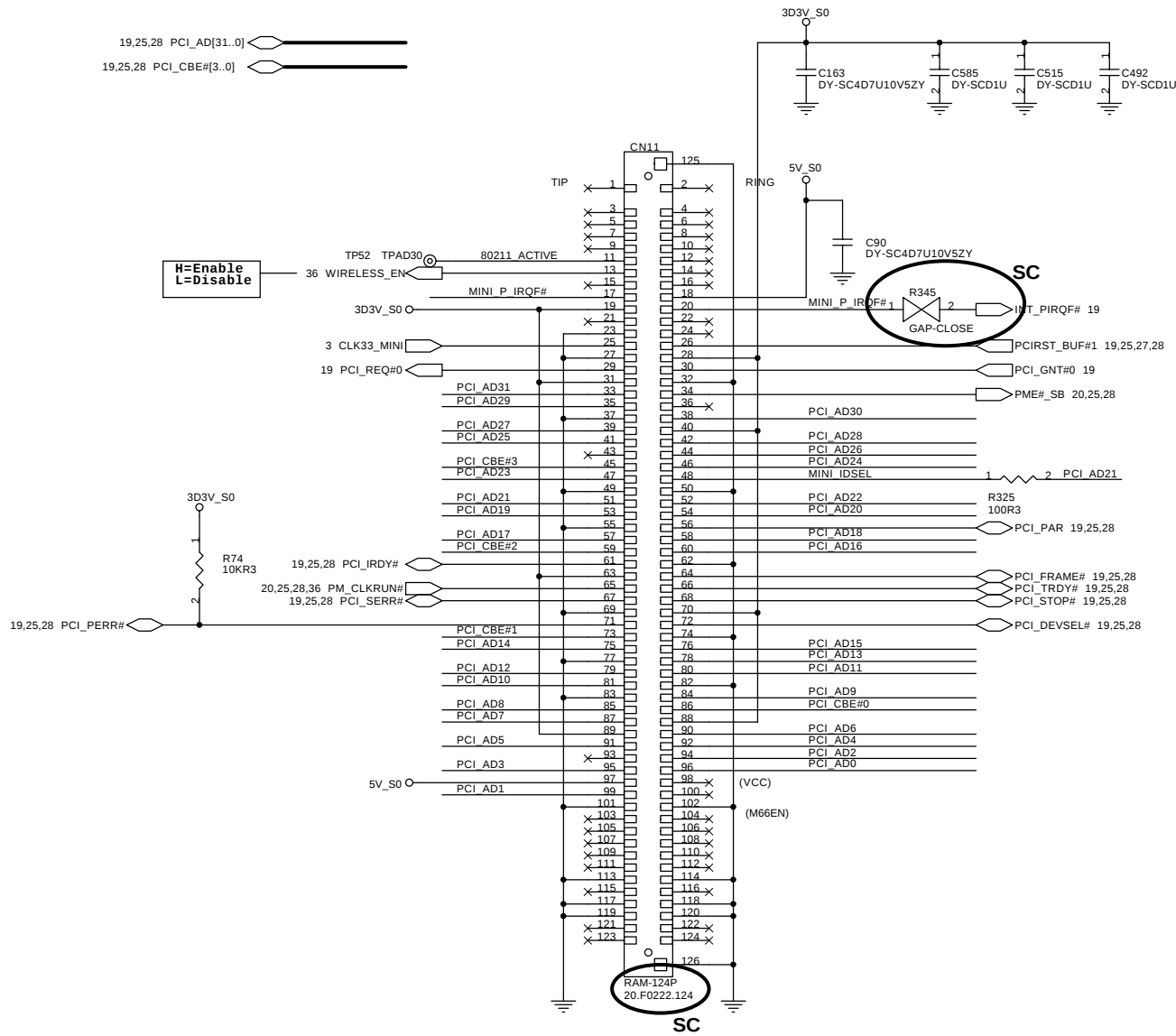


05/11
 For VIA suggest.
 VT6103L need 2U
 capacitor for PHYRST#

SB



MINI-PCI

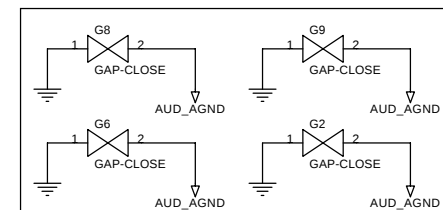
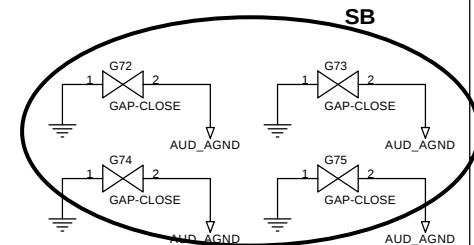
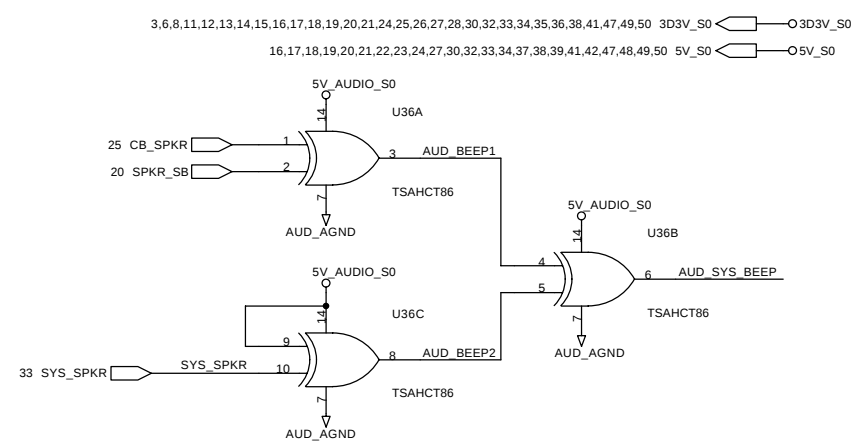


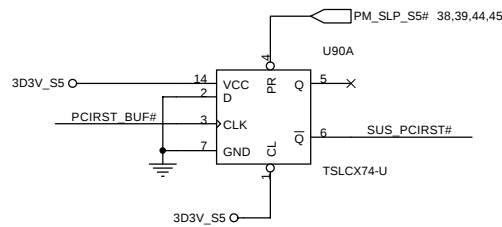
3,6,8,11,12,13,14,15,16,17,18,19,20,21,24,25,26,27,28,31,32,33,34,35,36,38,41,47,49,50 3D3V_S0

16,17,18,19,20,21,22,23,24,27,31,32,33,34,37,38,39,41,42,47,48,49,50 5V_S0

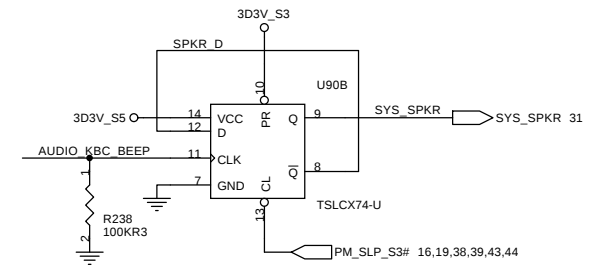
Title		MINI-PCI	
Size	Document Number	Rev	
A3	EGRET	SC	
Date: Friday, July 23, 2004		Sheet	30 of 50

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

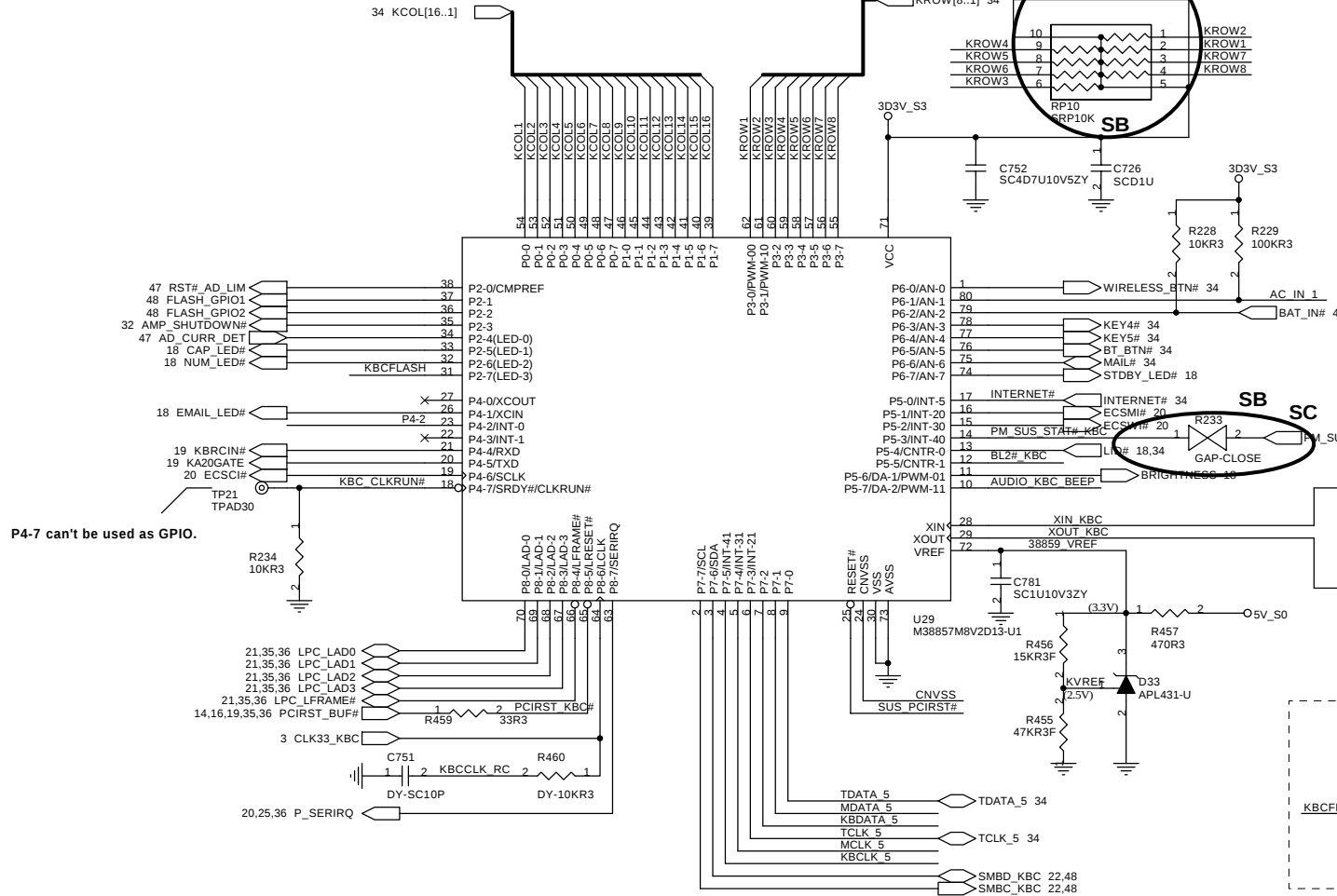




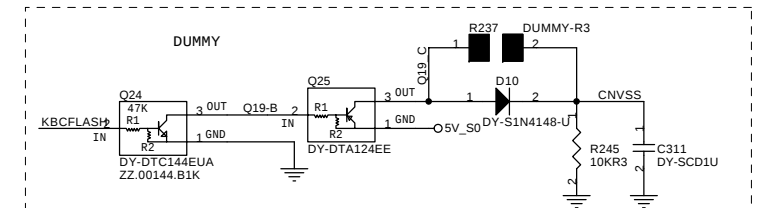
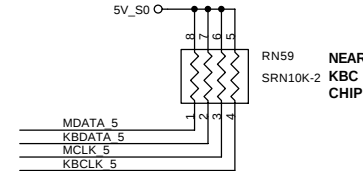
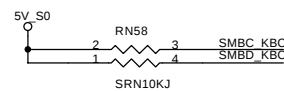
3,6,8,11,12,13,14,15,16,17,18,19,20,21,24,25,26,27,28,30,31,32,34,35,36,38,41,47,49,50 3D3V_S0
16,17,18,19,20,21,22,23,24,27,30,31,32,34,37,38,39,41,42,47,48,49,50 5V_S0
18,34,38,50 3D3V_S3

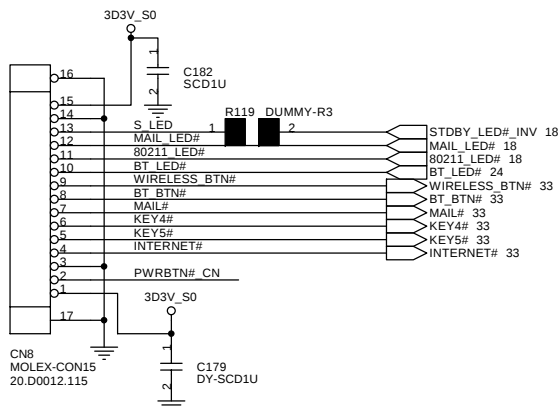


5/12 By Review Meeting

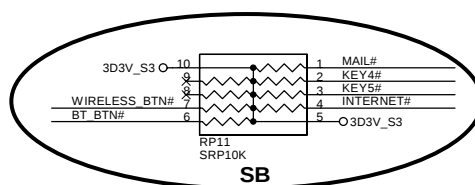
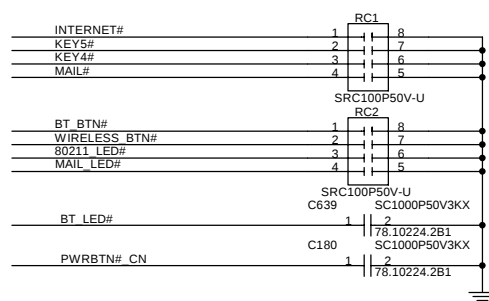
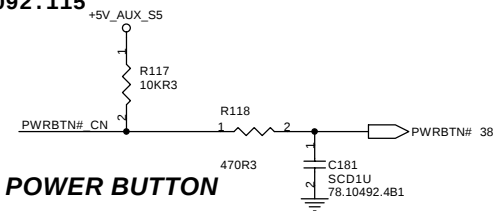


P/N: 85.49S01.001

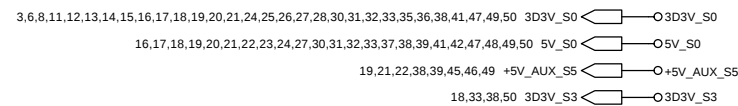




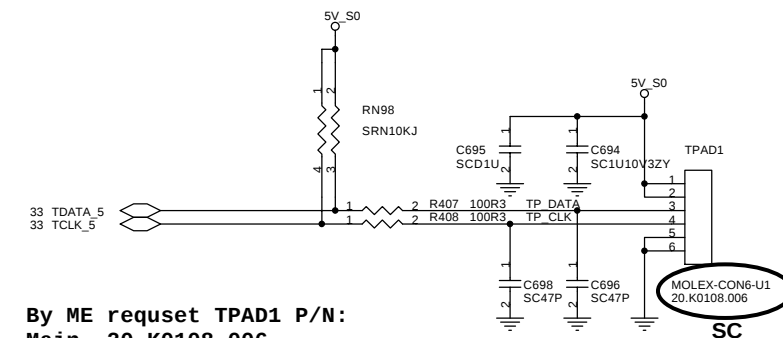
By ME request CN8 P/N:
Main 20.D0012.115
Second 20.D0092.115



Launch Board CONN



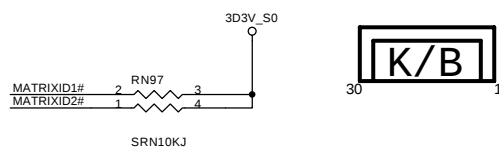
Cover Up Switch



By ME request TPAD1 P/N:
Main 20.K0108.006
Second 20.K0021.006

TOUCH PAD

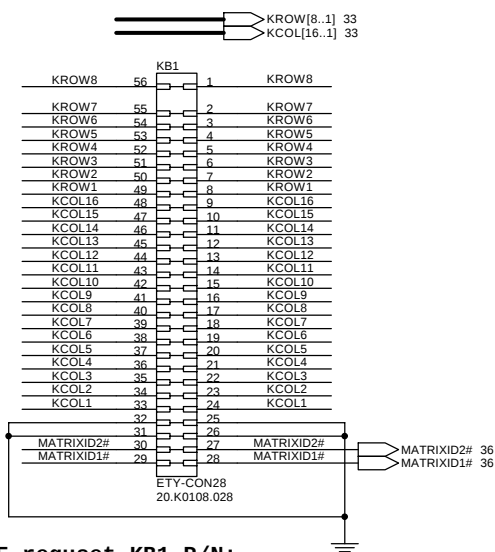
Internal KeyBoard CONN



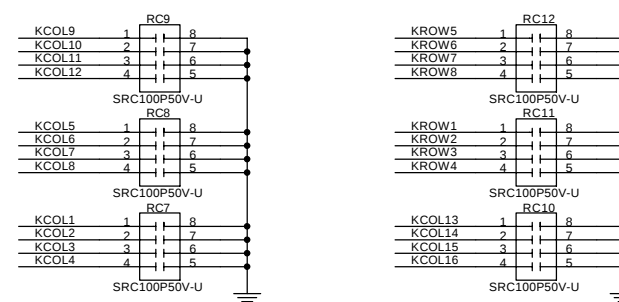
Keyboard matrix	(from vendor)			
	US	Jap	Eur	Other

Low Bit MATRIXID1# 1 1 0 0
High Bit MATRIXID2# 1 0 1 0

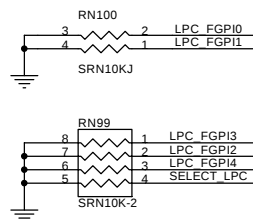
By ME request KB1 P/N:
Main 20.K0108.028
Second 20.K0021.028



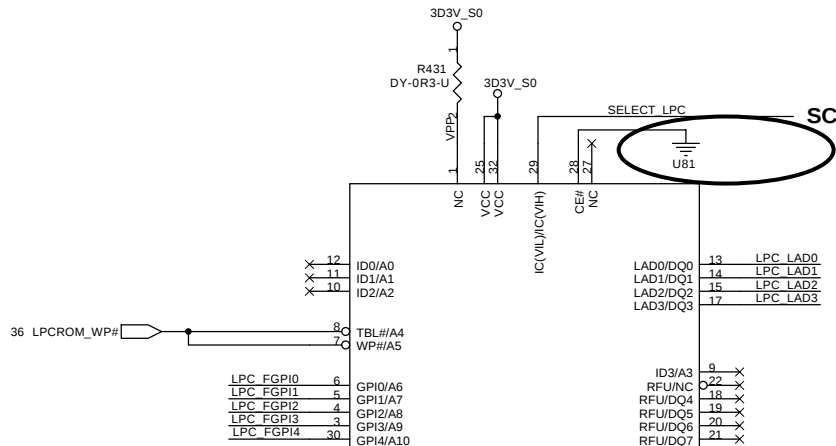
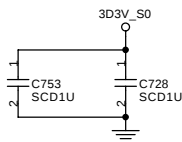
EMI Bypass cap.



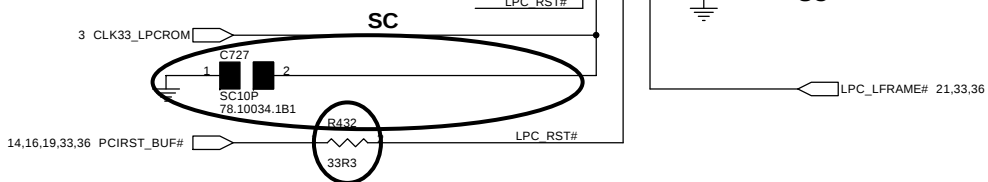
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
LAUNCH / TOUCHPAD / KB CONN	
Size	Document Number
A3	EGRET
Date: Friday, July 23, 2004	Sheet 34 of 50

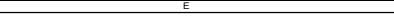
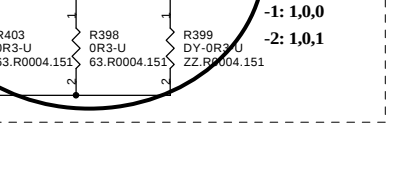
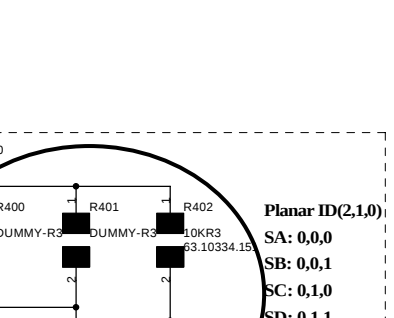
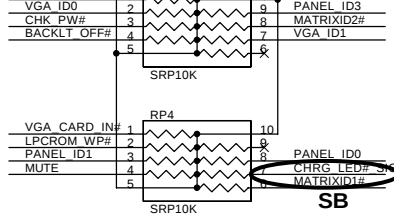
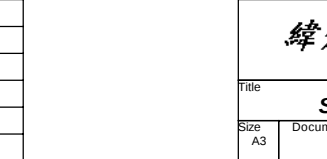
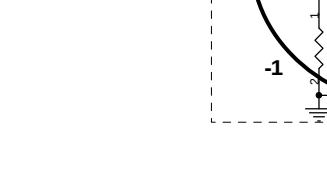
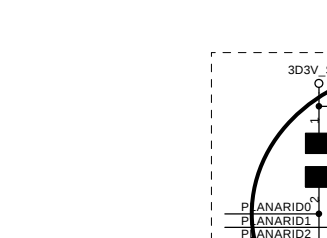
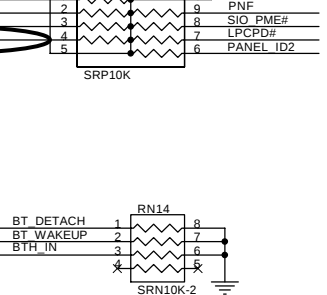
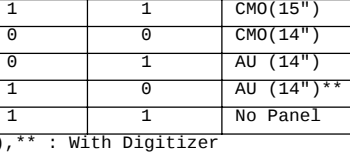
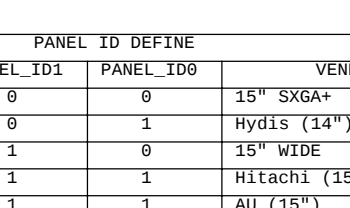
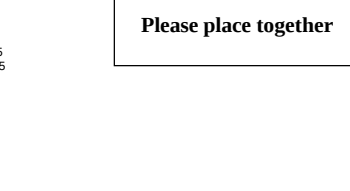
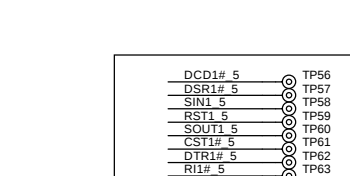
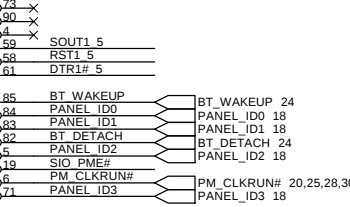
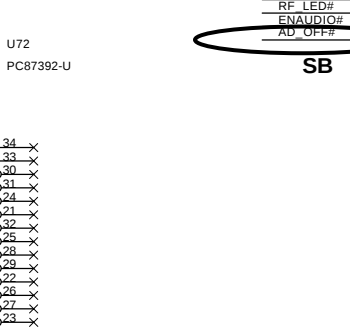
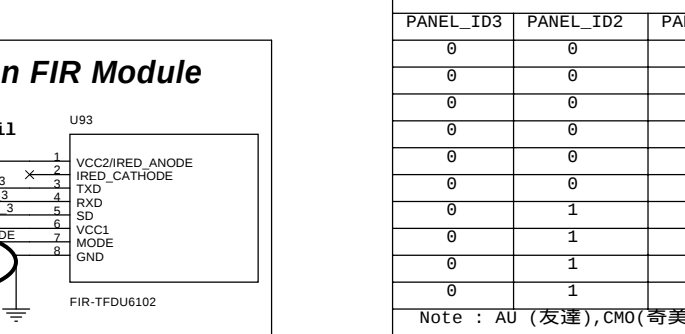
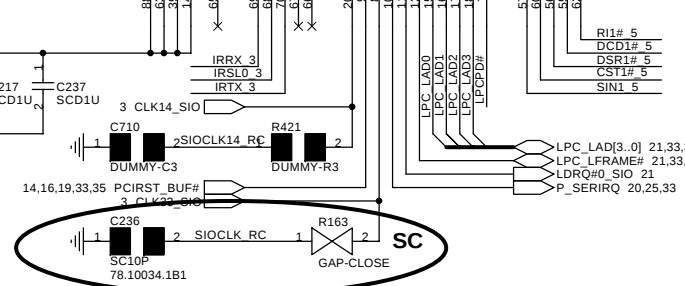
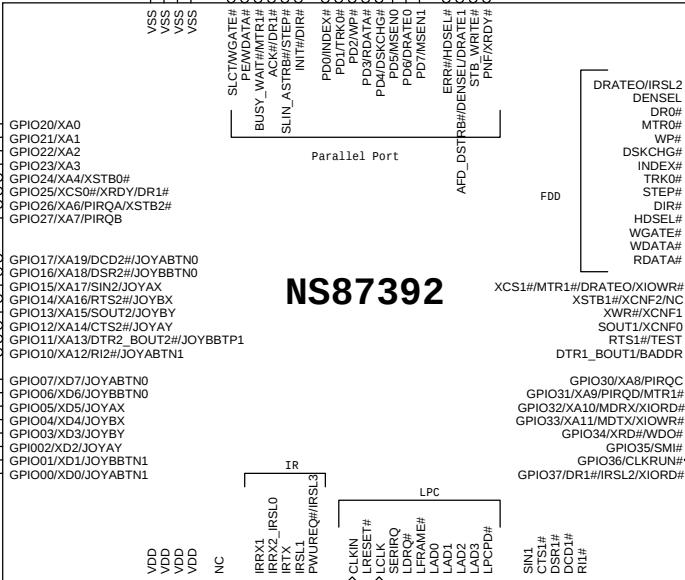
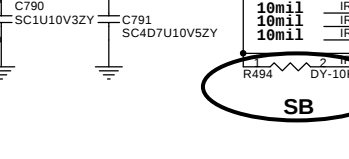
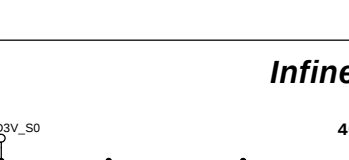
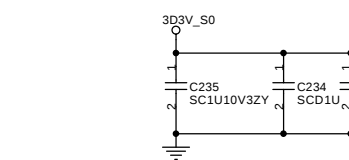
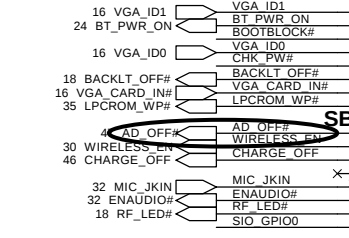
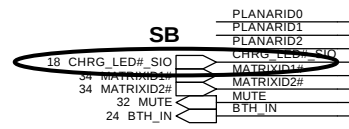
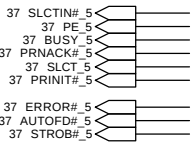


21,33,36 LPC_LAD[3..0]

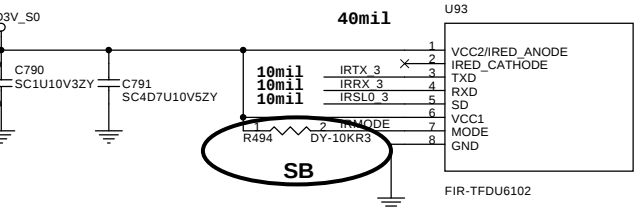


PLCC32 Socket P/N:
SSKT3262.10002.032
SSKT32 62.10005.032
LPC ROM:
SST49LF040 72.49040.A03
Winbond W39V040AP 72.39040.A03





Infineon FIR Module



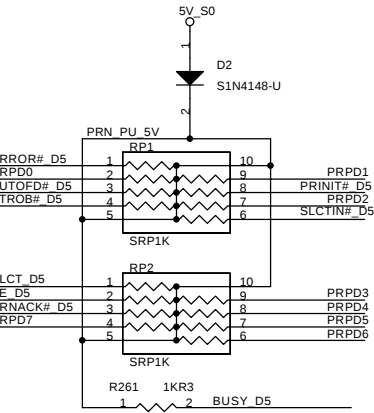
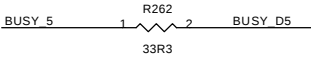
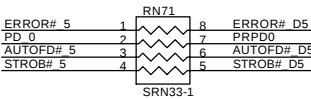
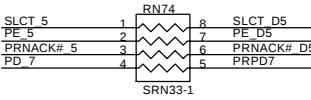
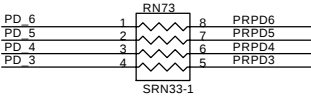
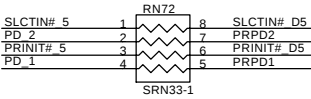
PANEL ID DEFINE				
PANEL_ID3	PANEL_ID2	PANEL_ID1	PANEL_ID0	VENDORS
0	0	0	0	15" SXGA+
0	0	0	1	Hydis (14")SPWG
0	0	1	0	15" WIDE
0	0	1	1	Hitachi (15")
0	0	1	1	AU (15")
0	1	0	0	CM0(15")
0	1	0	0	CM0(14")
0	1	0	1	AU (14")
0	1	1	0	AU (14")**
0	1	1	1	No Panel

Note : AU (友達),CM0(奇美),** : With Digitizer

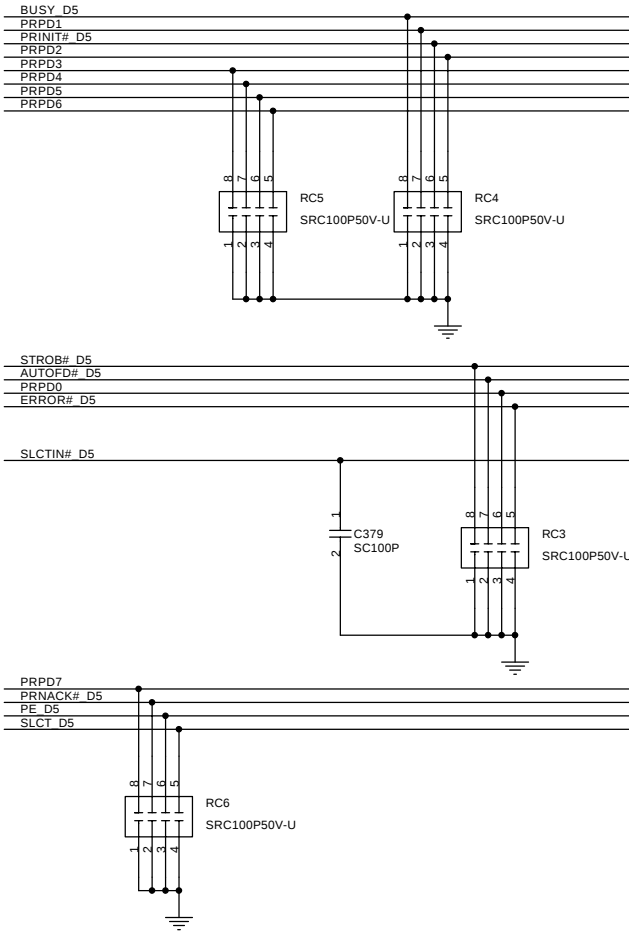
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PRINTER PORT



CHECK PULL HIGH



16,17,18,19,20,21,22,23,24,27,30,31,32,33,34,38,39,41,42,47,48,49,50 5V_S0 05V_S0

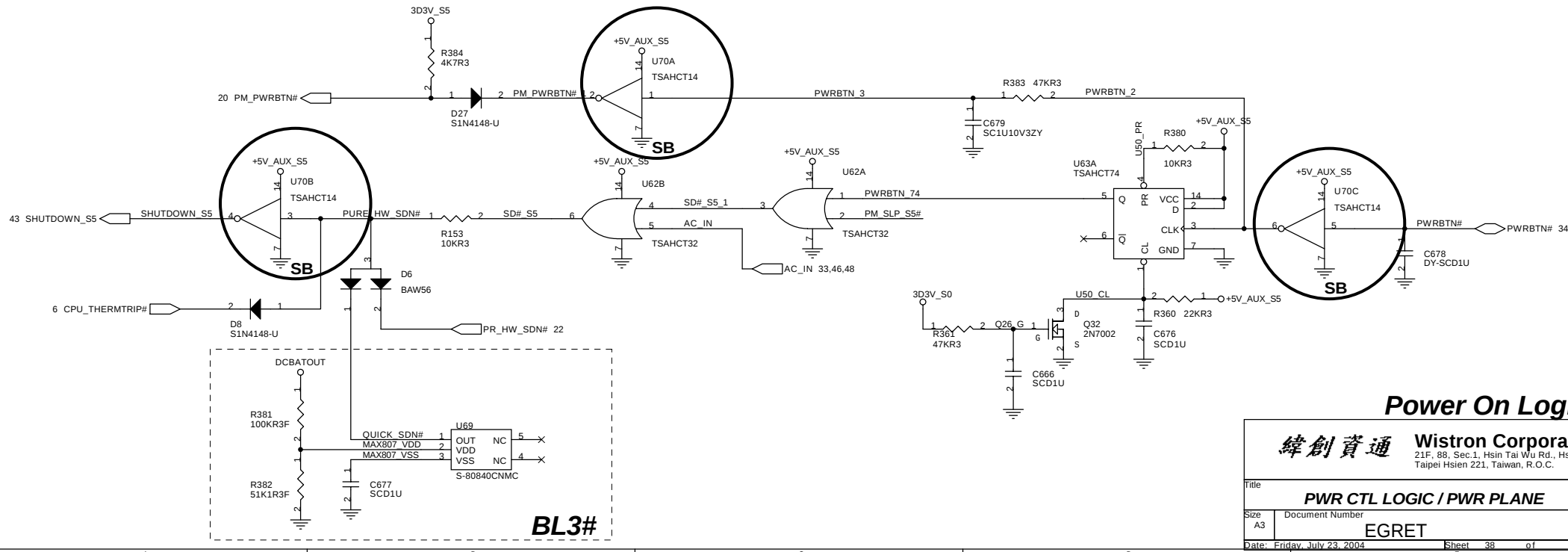
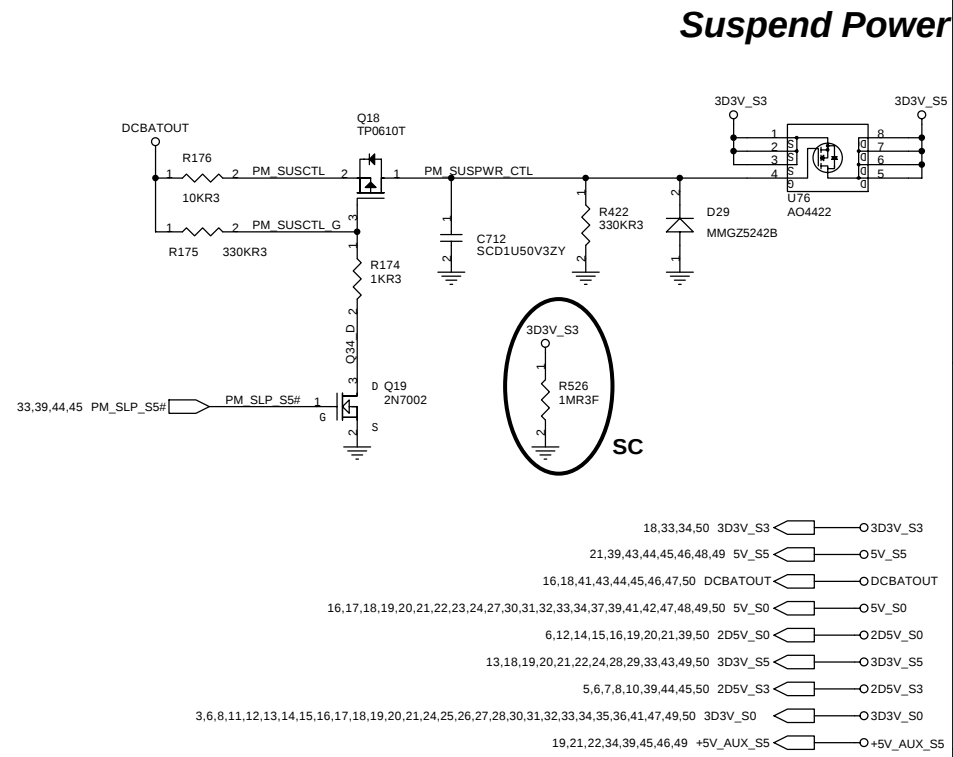
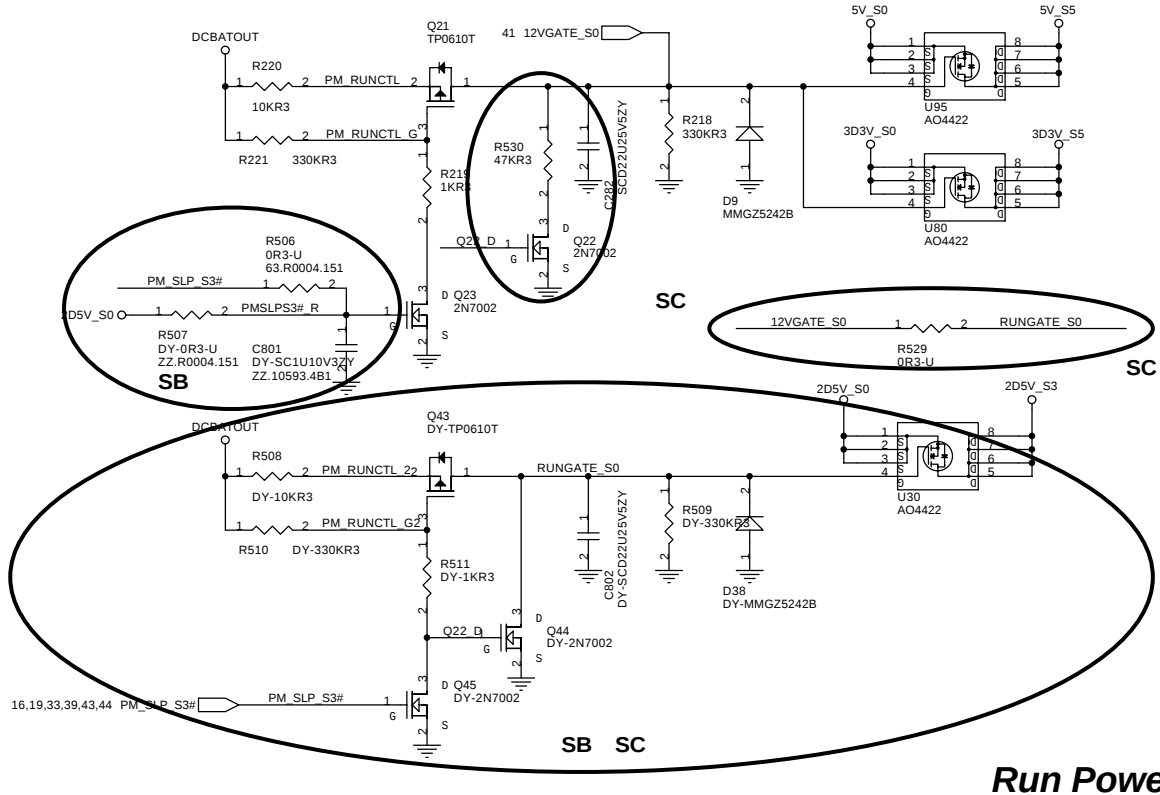
FROM SIO

- SLCT_5 36
- PE_5 36
- PRNACK#_5 36
- ERROR#_5 36
- PRINIT#_5 36
- SLCTIN#_5 36
- AUTOFD#_5 36
- STROB#_5 36
- BUSY_5 36

By ME request PRT1 P/N:
Main 20.B0030.A25
Second 20.B0028.L01

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Taipei Hsien 221, Taiwan, R.O.C.

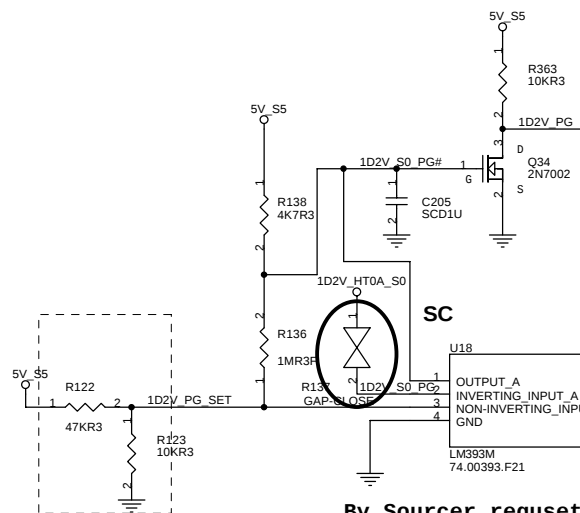
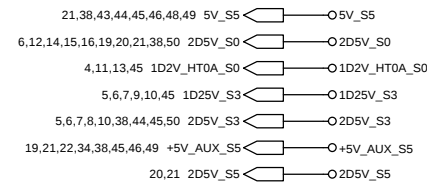
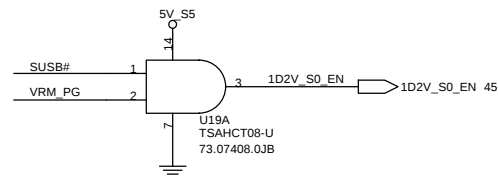
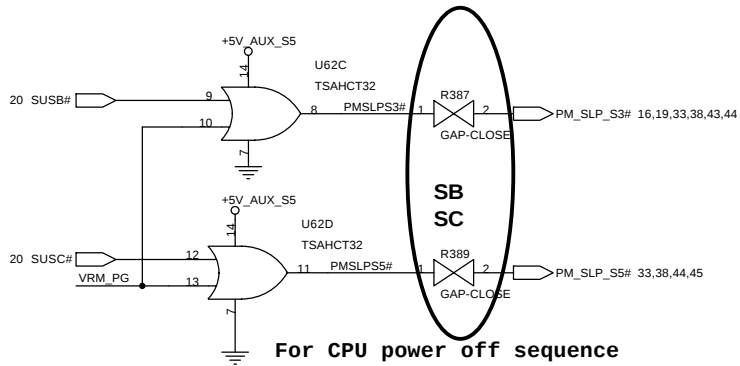
Title			
Printer PORT			
Size	Document Number		Rev
A3	EGRET		SC
Date: Friday, July 23, 2004		Sheet 37 of 50	



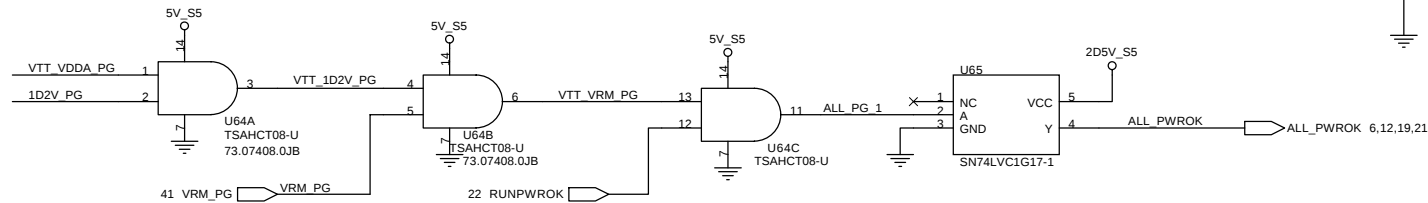
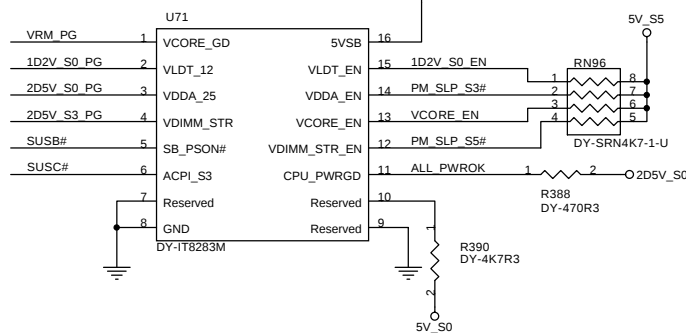
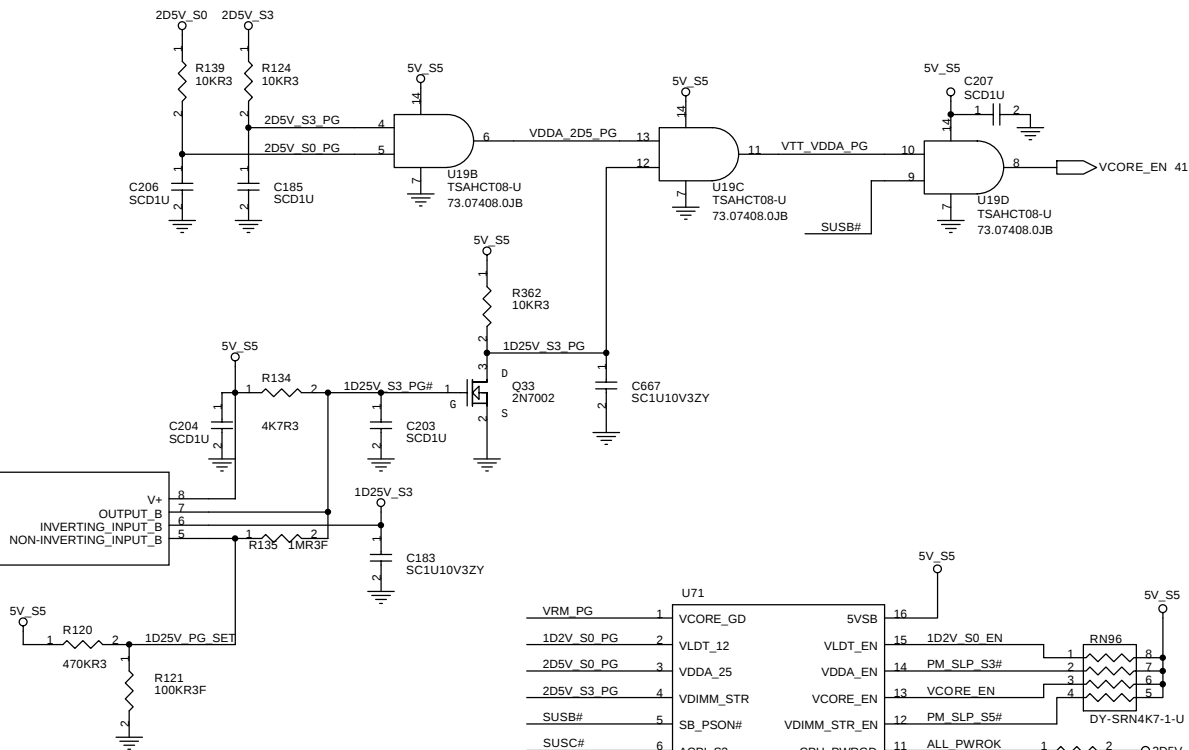
Power On Logic

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Taipei Hsien 221, Taiwan, R.O.C.

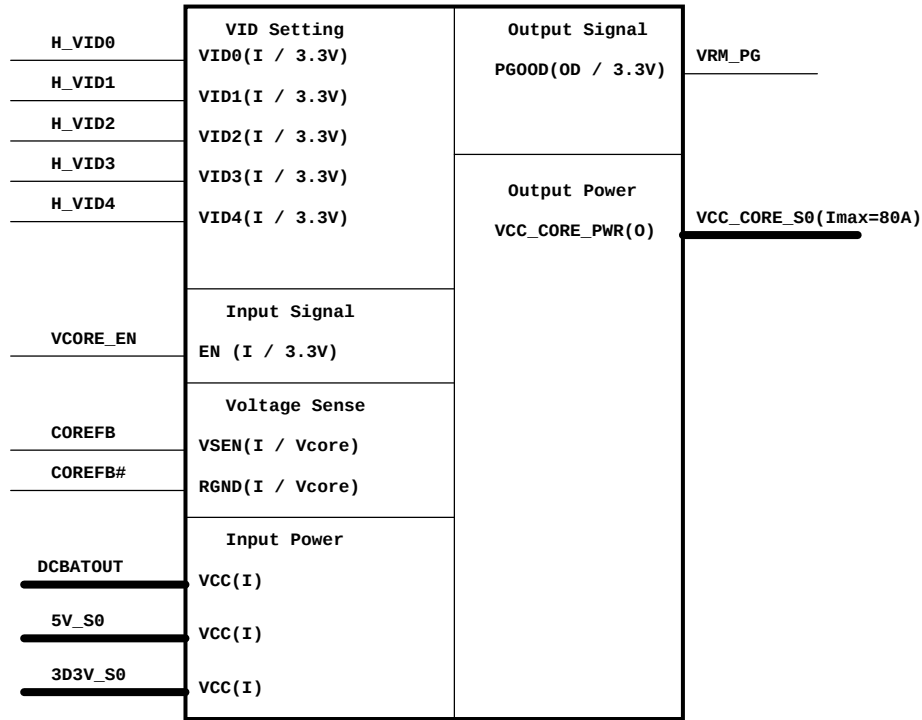
Title		
PWR CTL LOGIC / PWR PLANE		
Size A3	Document Number EGRET	Rev SC
Date: Friday, July 23, 2004	Sheet 38	of 50



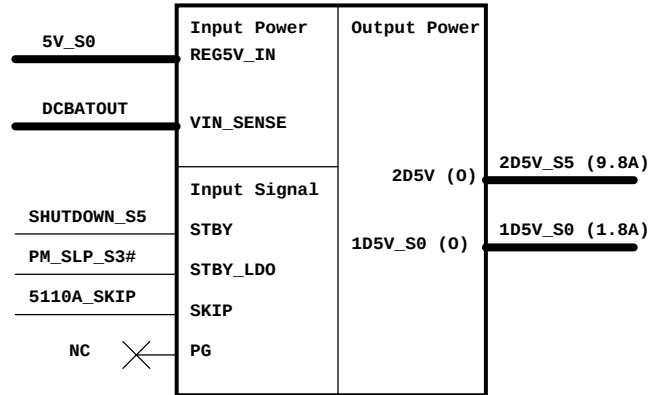
By Sourcer request change P/N:
From 74.00393.D21
To 74.00393.F21



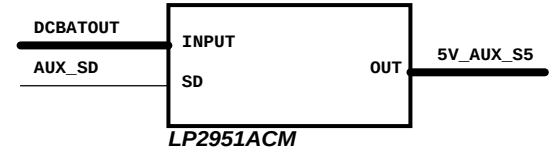
CPU_CORE
Intersil 6559CR + ISL6209CB*2



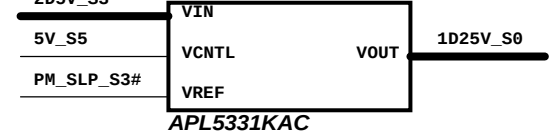
TI TPS5110
2D5V/1D5V



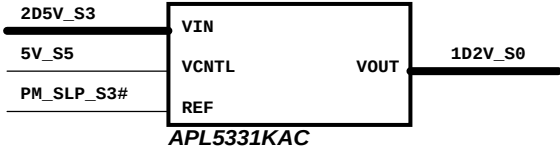
5V_AUX_S5



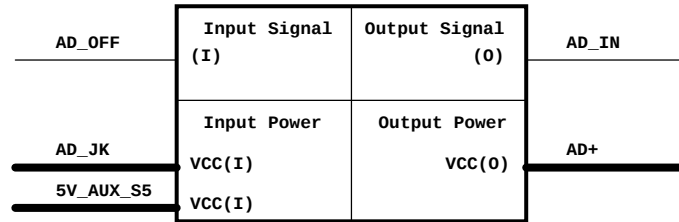
1D25V_S3



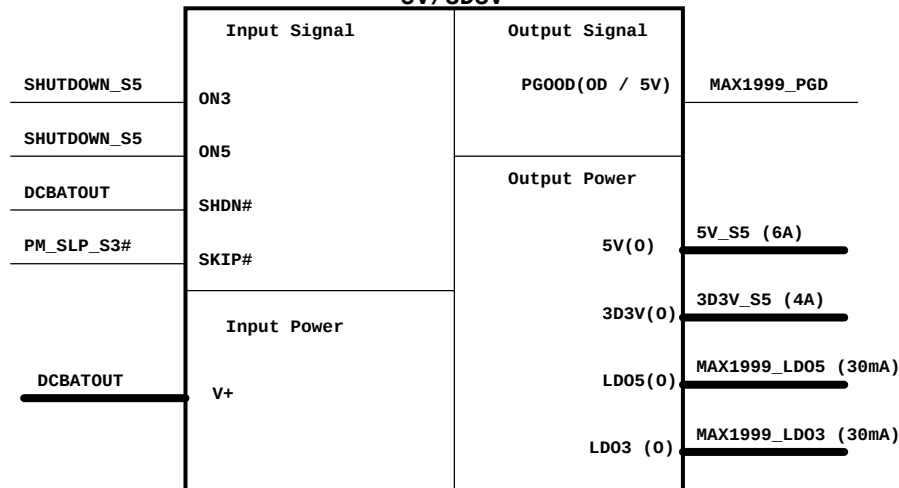
1D2V_S0



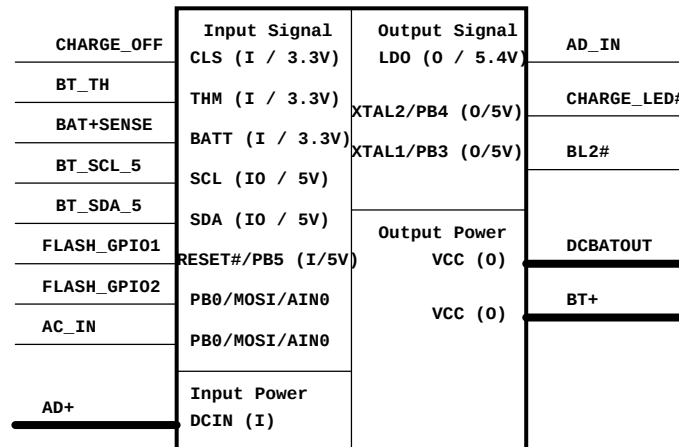
Adapter



Max1999
5V/3D3V



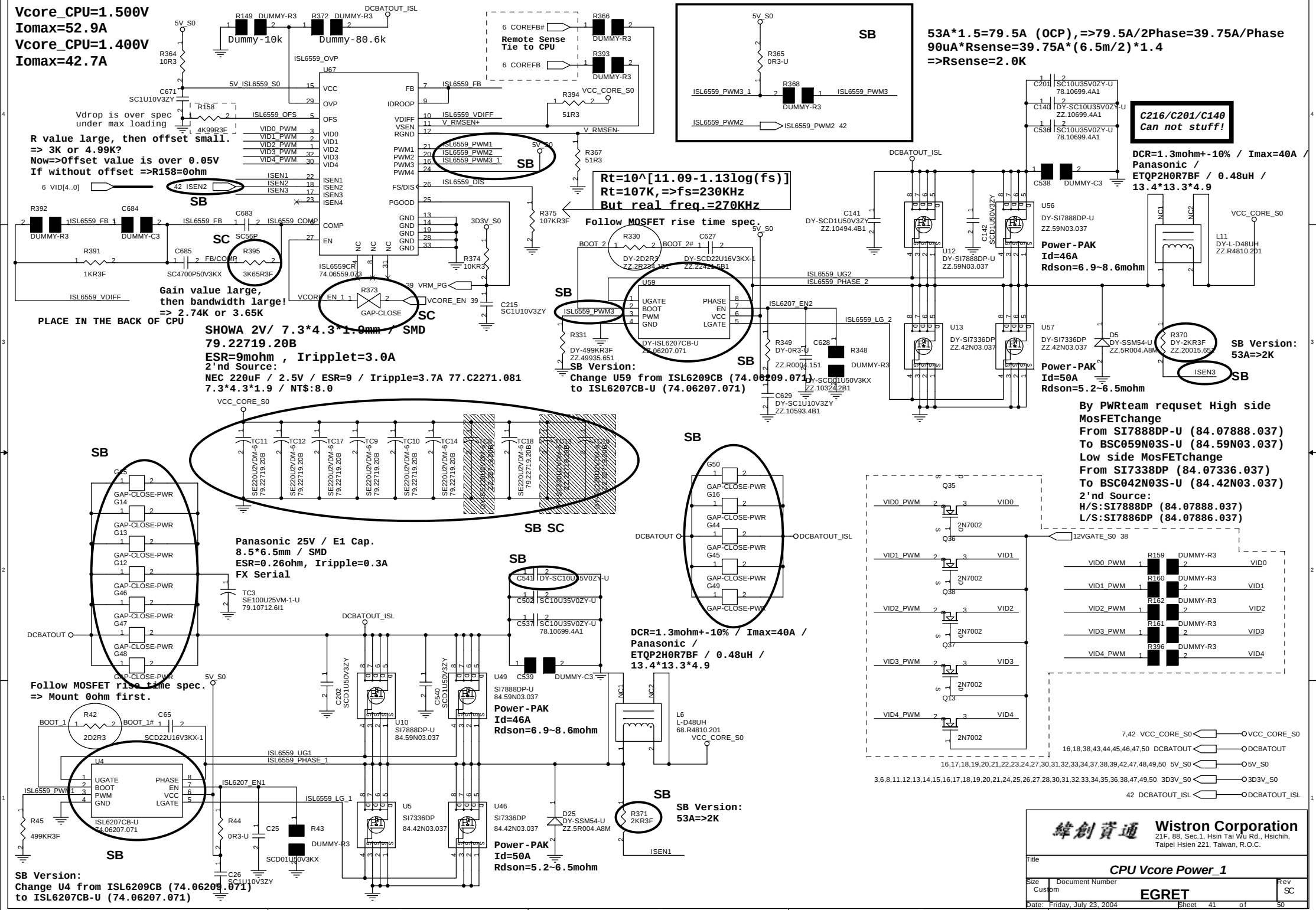
Charger_Max1645 + Tiny12



緯創資通

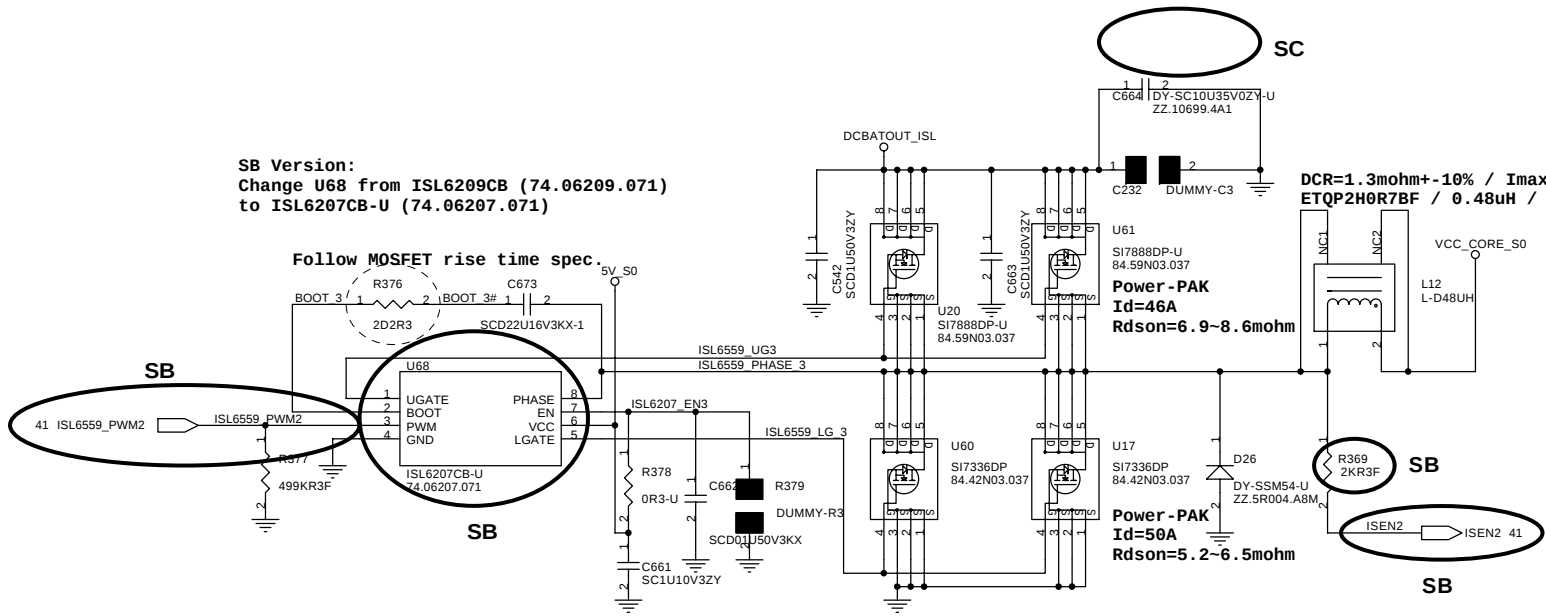
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Taipei Hsien 221, Taiwan, R.O.C.

Vcore_CPU=1.500V
Iomax=52.9A
Vcore_CPU=1.400V
Iomax=42.7A



SB Version:
Change U68 from ISL6209CB (74.06209.071)
to ISL6207CB-U (74.06207.071)

Follow MOSFET rise time spec.



By PWRteam request High side
MosFETchange
From SI7888DP-U (84.07888.037)
To BSC059N03S-U (84.59N03.037)
Low side MosFETchange
From SI7338DP (84.07336.037)
To BSC042N03S-U (84.42N03.037)

TABLE 1. VOLTAGE IDENTIFICATION CODES
VID4 VID3 VID2 VID1 VID0 DAC

0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

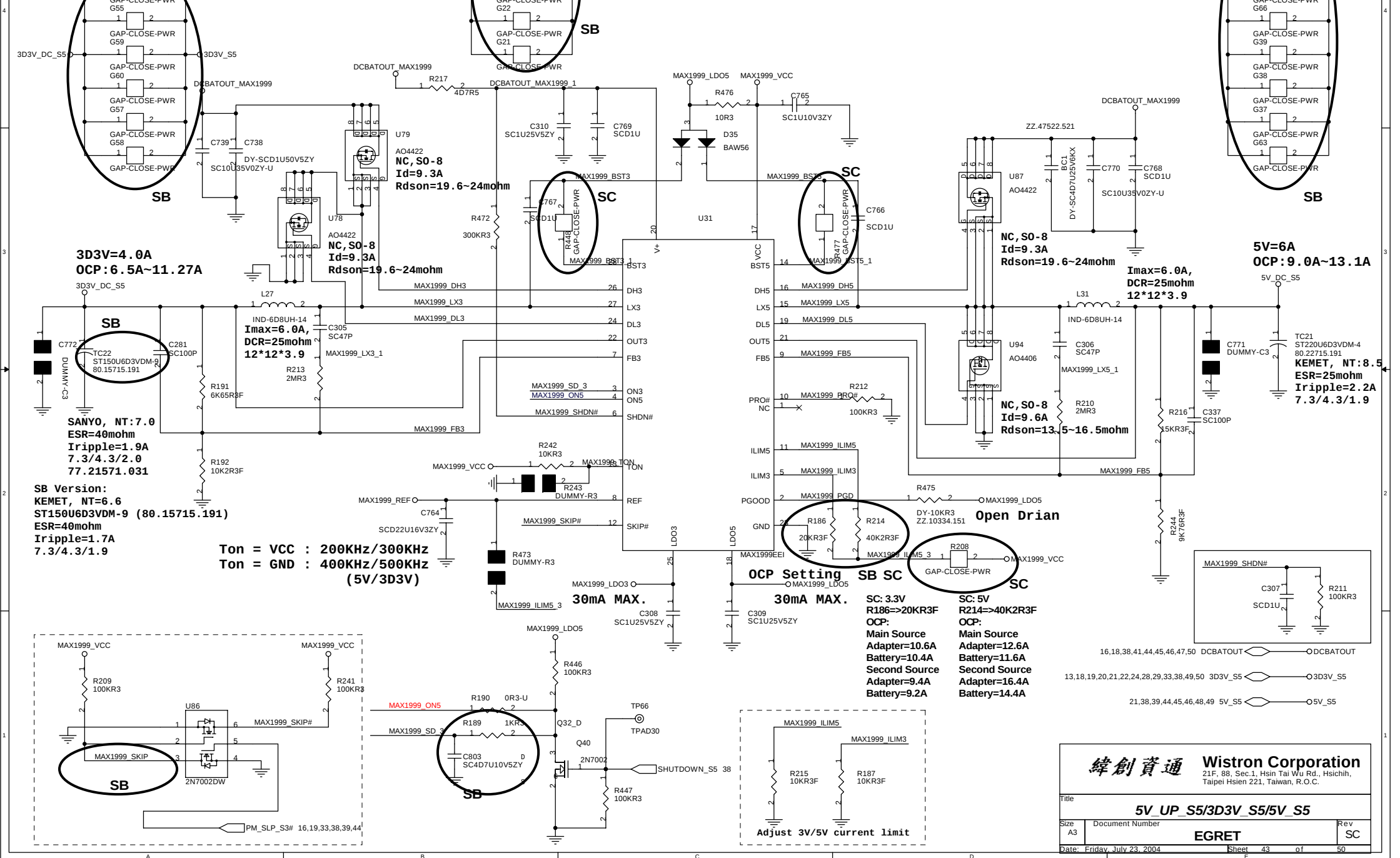
41 DCBATOUT_ISL

7,41 VCC_CORE_S0

16,17,18,19,20,21,22,23,24,27,30,31,32,33,34,37,38,39,41,47,48,49,50 5V_S0

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Taipei Hsien 221, Taiwan, R.O.C.

SYSTEM DC/DC
3D3V_S5/5V_S5

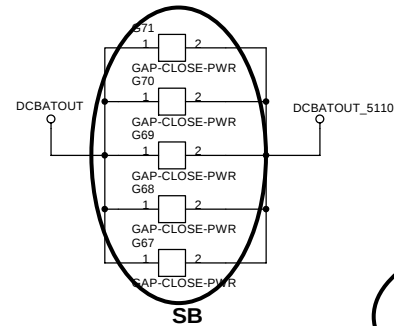


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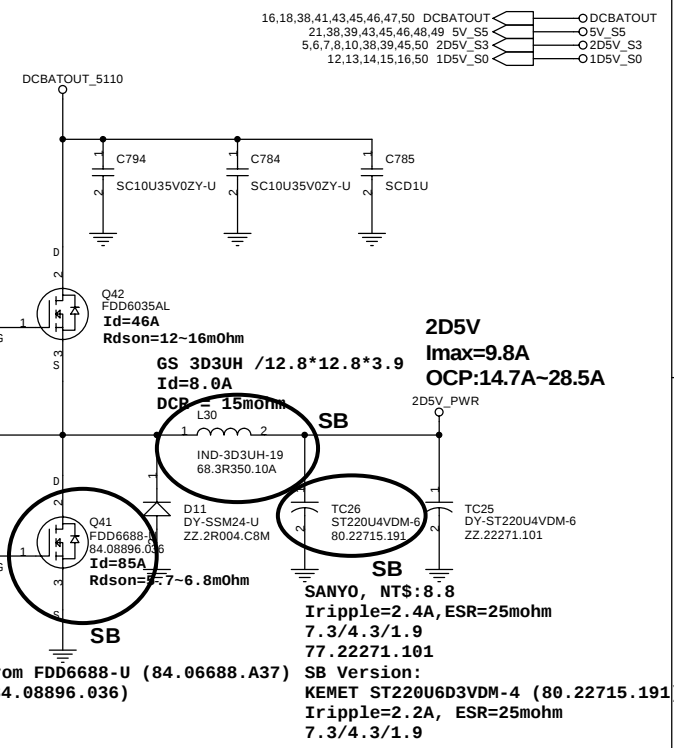
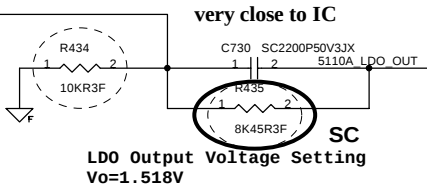
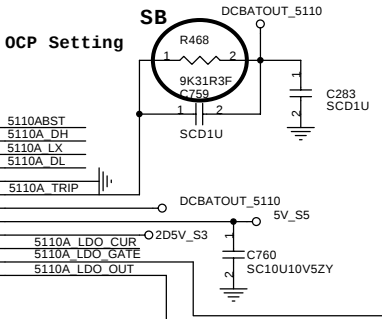
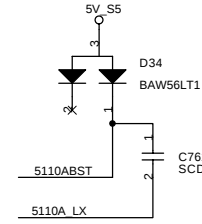
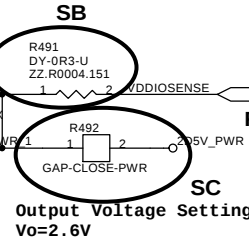
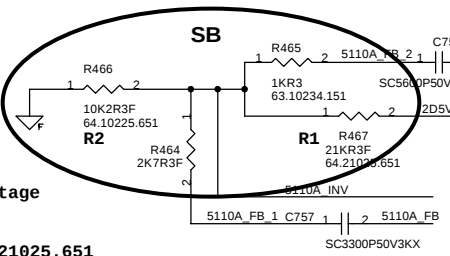
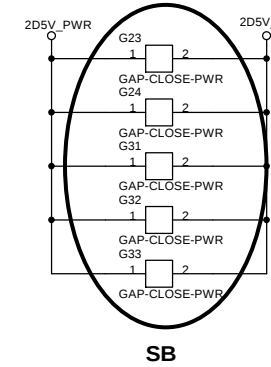
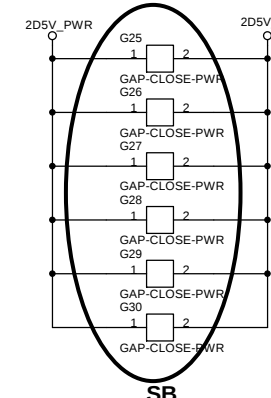
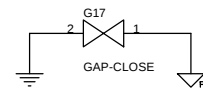
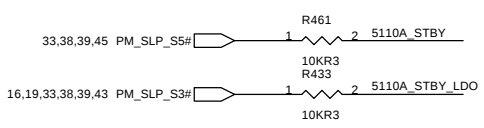
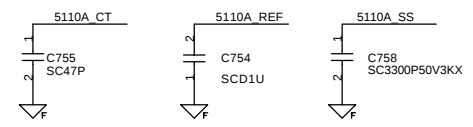
Title			
5V_UP_S5/3D3V_S5/5V_S5			
Size A3	Document Number		Rev
	EGRET		SC
Date: Friday, July 23, 2004	Sheet	43	of 50

TI TPS5110 for 2.5V and 1.5V

CT = 47pF/300KHz
2D5V_S5: 9.8Amax , OCP>14.7A
1D5V_S3: 1.8Amax , OCP>3.3A



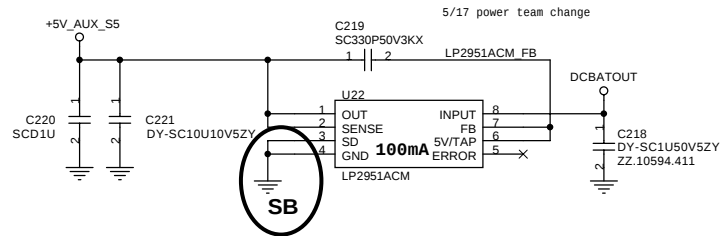
Change Output Voltage from 2.5V to 2.6V (support DDR400)
R467 = 21KR3F 64.21025.651
R466 = 10K2R3F 64.10225.651



SB Version:
KEMET, NT:5.7, B2 size
ST100U4VBM-1 (80.10716.321)
Iripple=1.1A, ESR=70mohm

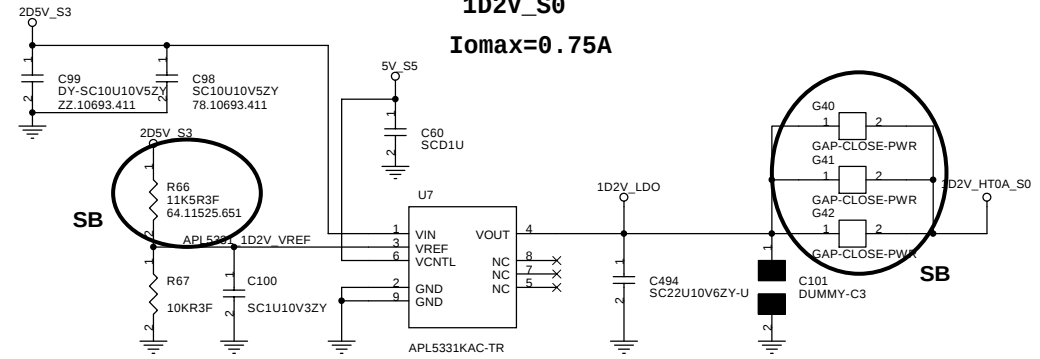
1D5V
Imax=1.8A
OCP>3.3A

5V_AUX_S5



1D2V_S0

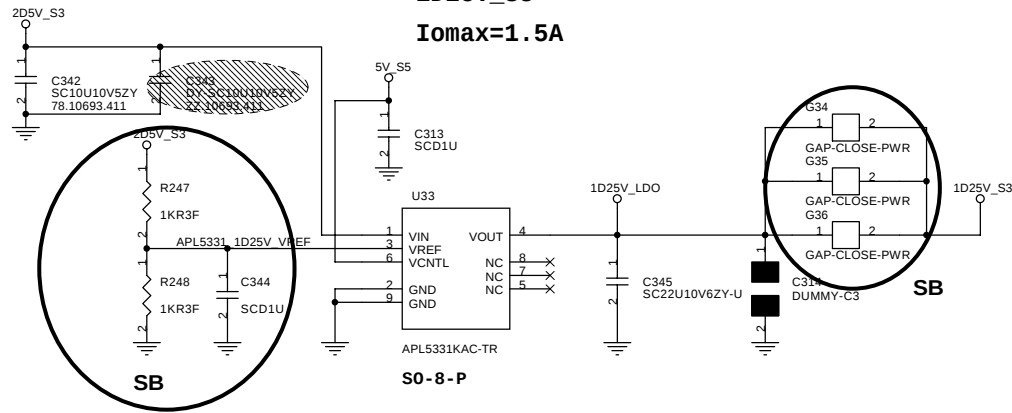
Iomax=0.75A



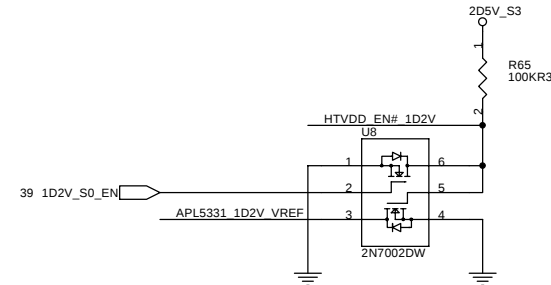
S0-8-P

1D25V_S3

Iomax=1.5A



S0-8-P



4,11,13,39 1D2V_HT0A_S0 → 1D2V_HT0A_S0

16,18,38,41,43,44,46,47,50 DCBATOUT → DCBATOUT

19,21,22,34,38,39,46,49 +5V_AUX_S5 → +5V_AUX_S5

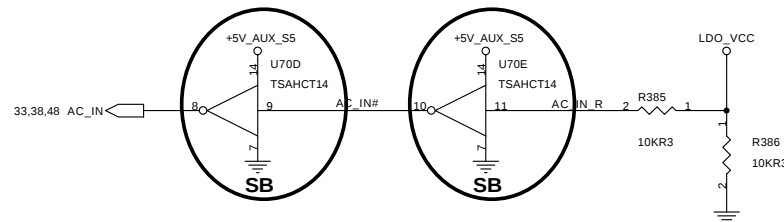
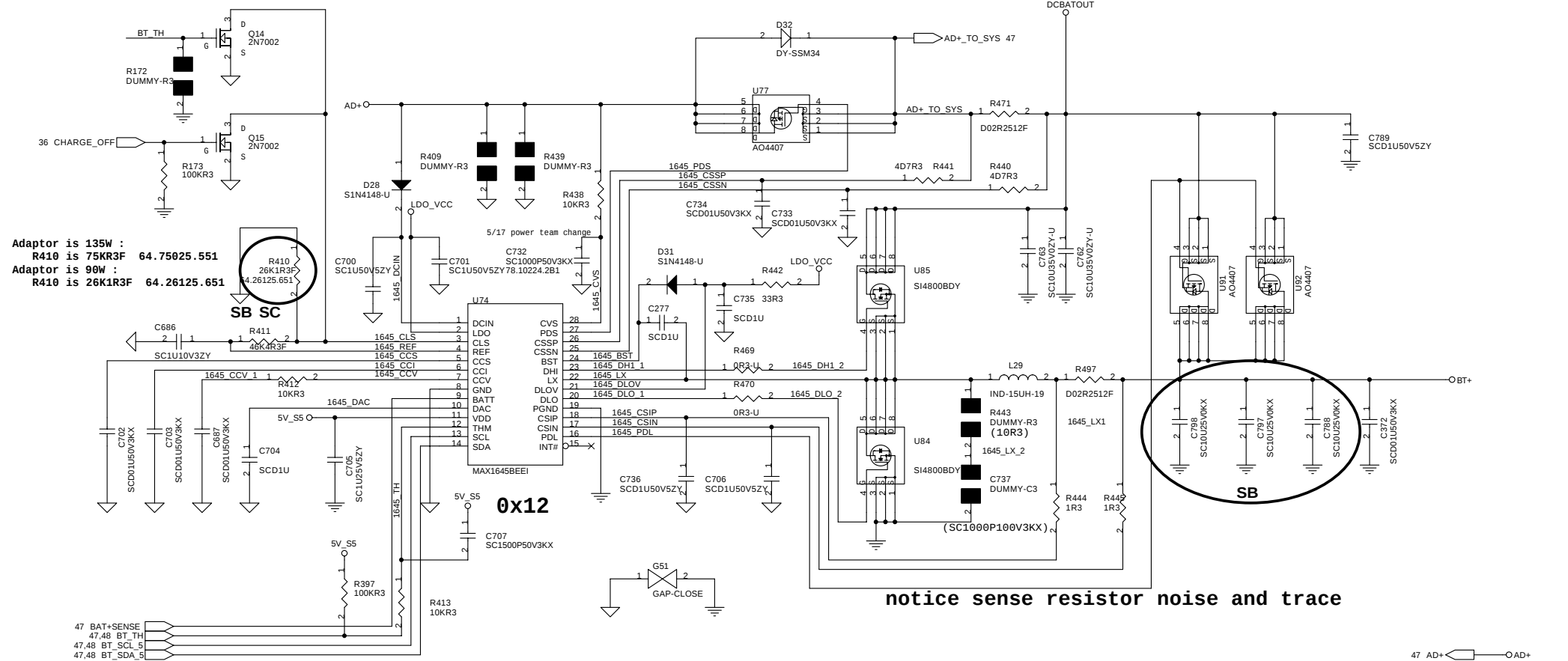
21,38,39,43,44,46,48,49 5V_S5 → 5V_S5

5,6,7,8,10,38,39,44,50 2D5V_S3 → 2D5V_S3

5,6,7,9,10,39 1D25V_S3 → 1D25V_S3

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Title		
1D25V_LDO/3V_AUX/5V_AUX		
Size	Document Number	Rev
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Date: Friday, July 23, 2004		
Sheet 45 of 50		

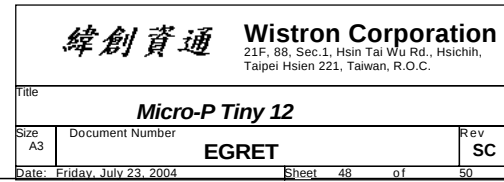
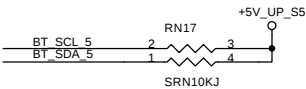
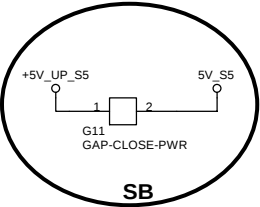


Li-ion =>8 Cells (4S2P*2=16.8V)
Ni-Mh =>8 Cells (8*1.8=14.4V)

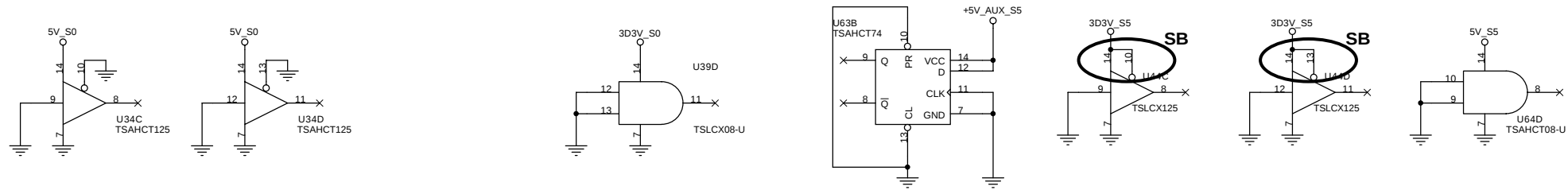
Low => Li-ion
(3.3A=2400mAH*2*0.7C)
High => Ni-MH
(2.5A=4800mAH*0.55C)

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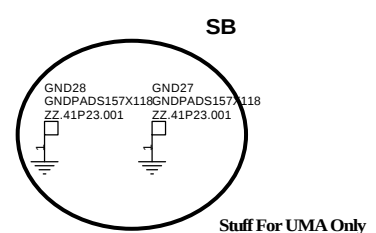
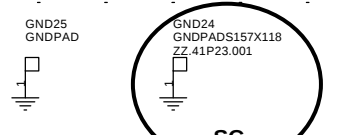
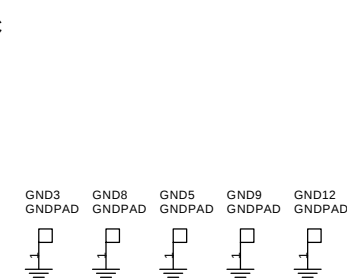
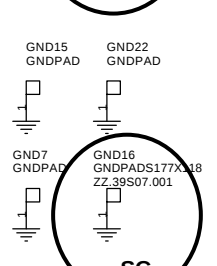
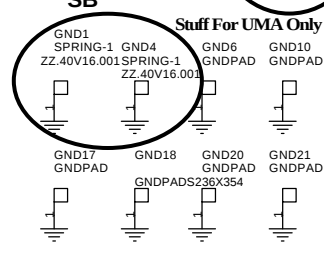
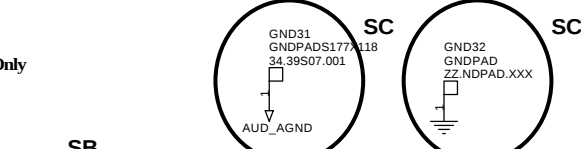
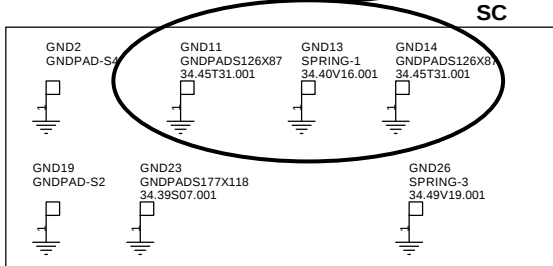
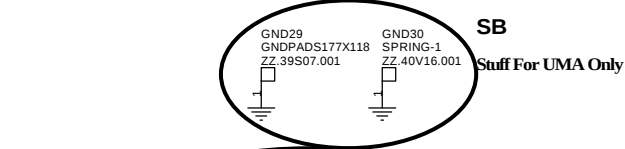
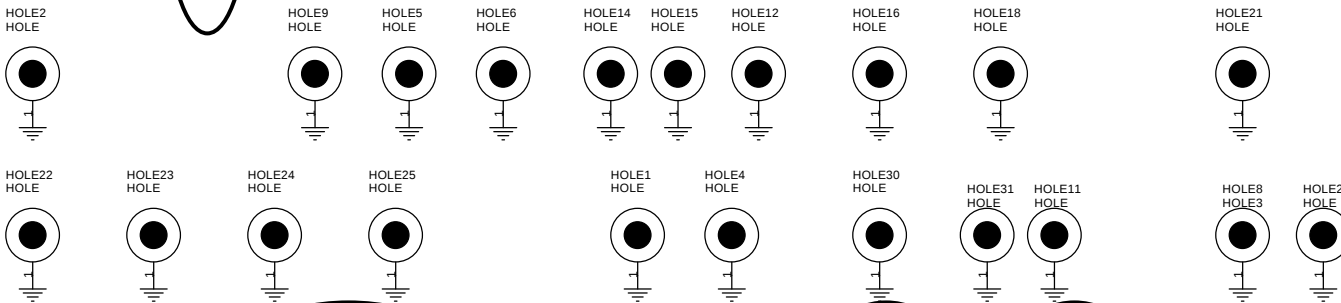
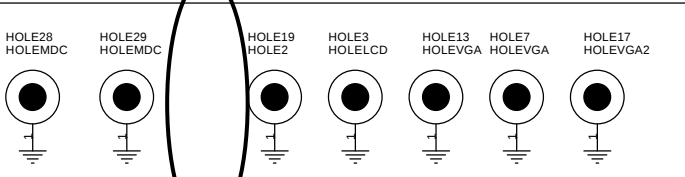
Title	CHARGER MAX1645		
Size	Document Number	EGRET	Rev
Custom			SC
Date:	Friday, July 23, 2004	Sheet 46 of 50	



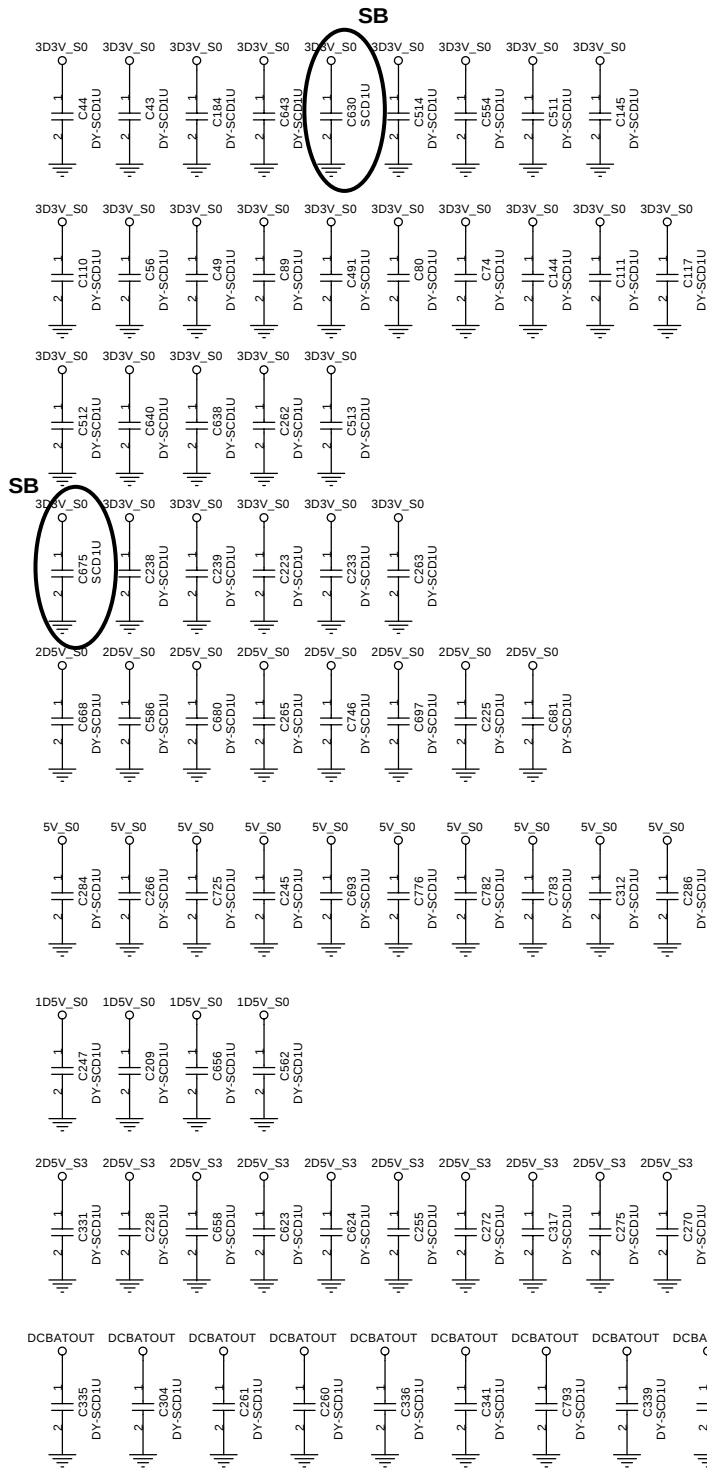
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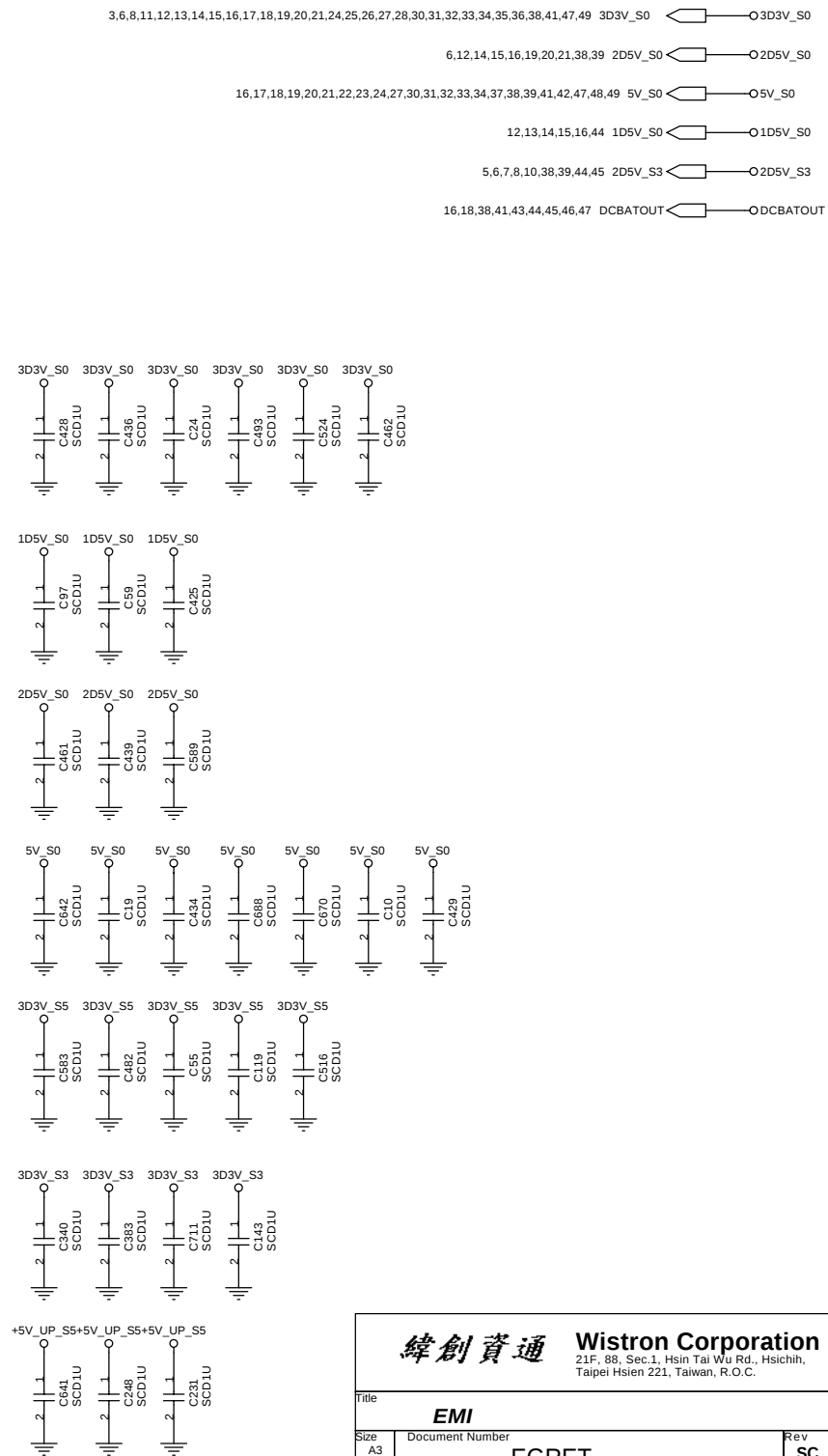
SB
SC



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Size A3	Document Number	Rev SC
EGRET		
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